FAIRCHILD
A Schlumberger Company

F6847
Video Display Generator

Microprocessor Product

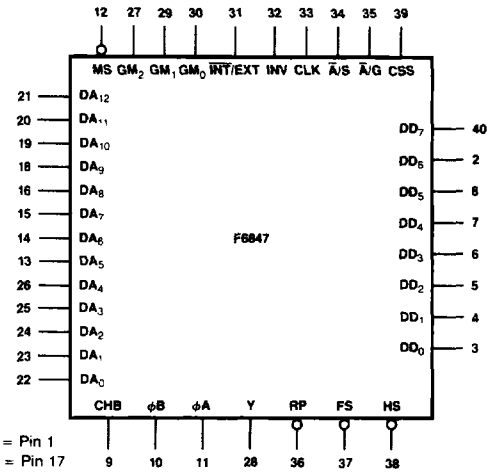
Description

The Fairchild F6847 Video Display Generator (VDG) provides a means of interfacing the Fairchild F6800 microprocessor family (or similar products) to a commercially available color or black-and-white television receiver. Applications of the VDG include video games, bioengineering displays, education, communications, and any instance in which graphics are required.

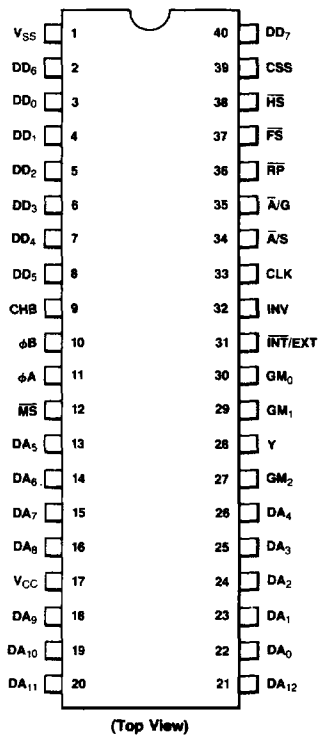
The VDG reads data from memory and produces a composite video signal that allows the generation of alphanumeric or graphic displays. The generated composite video may be up-modulated to either channel 3 or 4 by using a suitable rf modulator. The up-modulated signal is suitable for application to the antenna of a color TV. *Figure 1* illustrates a typical TV game application.

- **Generates Four Different Alphanumeric Display Modes and Eight Graphic Display Modes**
- **Compatible With the F6800 Family**
- **The Alphanumeric Modes Display 32 Characters per Line by 16 Lines.**
- **An Internal Multiplexer Allows the Use of Either the Internal ROM or an External Character Generator.**
- **An External Character Generator Can Be Used to Extend the Internal Character Set for "Limited Graphic" Shapes.**
- **One Display Mode Offers 8-Color 64 x 32 Density Graphics in an Alphanumeric Display Mode.**
- **One Display Mode Offers 4-Color 64 x 48 Density Graphics in an Alphanumeric Display Mode.**
- **All Alphanumeric Modes Have a Selectable Video Inverse.**
- **Generates Full Video Signal**
- **Generates R-Y and B-Y Signals for External Color Modulator**
- **Full Graphic Modes Offer 64 x 64, 128 x 64, 128 x 96, 128 x 192, or 256 x 192 Densities.**
- **Full Graphic Modes Allow 2-Color or 4-Color Data Structures.**
- **Full Graphic Modes Use One of Two 4-Color Sets or One of Two 2-Color Sets.**

Logic Symbol



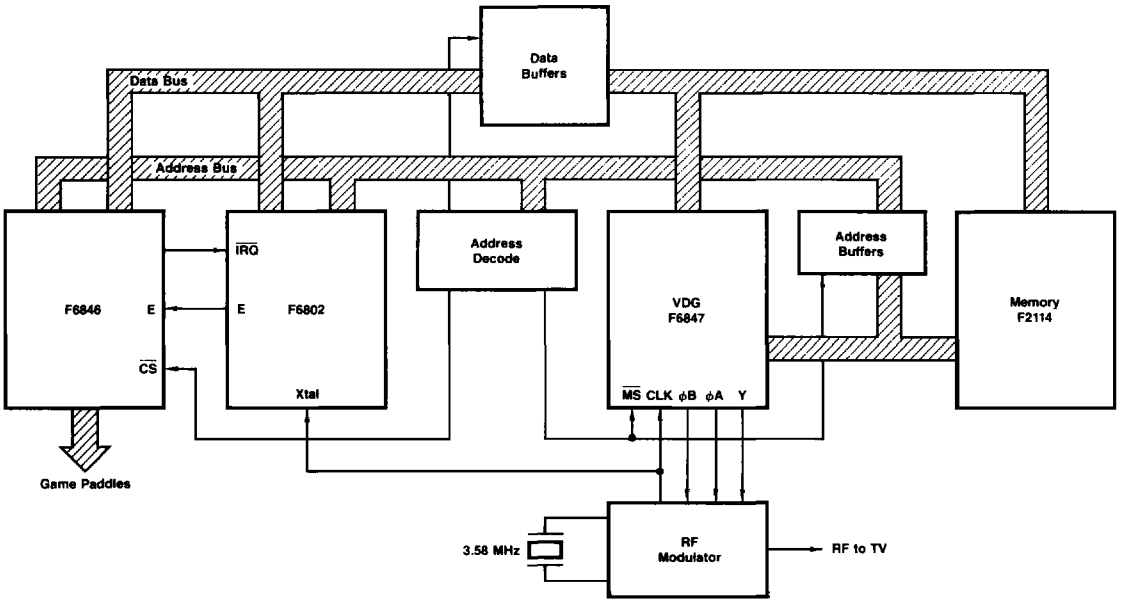
Connection Diagram
40-Pin DIP



(Top View)

5

Fig. 1. Block Diagram of Use of the VDG in a TV Game



Pin Functions

V_{CC}	+5 V
V_{SS}	Ground
CLK	Color burst clock 3.58 MHz (input)
$DA_0 - DA_{12}$	Address lines to display memory, high impedance during memory select (MS)
$DD_0 - DD_5$	Data from display memory RAM or ROM
DD_6, DD_7	Data from display memory in graphic mode; data also in alpha external mode; color data in alpha semigraphic-4 or -6 mode
ϕA, ϕB, Y	Chrominance and luminance analog (R-Y, B-Y, Y) output to rf modulator
CHB	Chroma Bias; reference ϕA and ϕB levels
$\overline{RP}$	Row Preset; output to provide timing for external character generator
$\overline{HS}$	Horizontal Sync; output to provide timing for external character generator
$\overline{INV}$	Inverts video in all alpha modes
$\overline{INT}$/EXT	Switches to external ROM in alpha mode and between alpha semigraphic-4 and alpha semigraphic-6 in semigraphics mode
$\overline{A}$/S	Alpha/Semigraphics; selects between alpha and semigraphics in alpha mode
$\overline{MS}$	Memory Select; forces VDG address buffers to high-impedance state
$\overline{A}$/G	Switches between alpha and graphic modes
$\overline{FS}$	Field Synchronization; goes low at bottom of active display area
CSS	Color Set Select; selects between two alpha display colors or between two color sets in semigraphics-6 and full graphics mode
$GM_0 - GM_2$	Graphic Mode Select; selects one of eight graphic modes

VDG Signal Descriptions

Address Outputs (DA_0 – DA_{12})
Thirteen address lines are used by the VDG to scan the display memory. The starting address of the display memory is located at the upper left corner of the display screen. As the television sweeps from left to right and top to bottom, the VDG increments the RAM display address. These lines are TTL-compatible and may be forced into a high-impedance state whenever the $\overline{MS}$ pin goes LOW.

Data Inputs (DD_0 – DD_7)
Eight TTL-compatible data lines are used to input data from the RAM to be processed by the VDG. The data is interpreted and transformed into luminance Y (pin 28) and color outputs ϕA and ϕB (pin 11 and pin 10).

Power Inputs
V_{CC} requires +5 volts. V_{SS} requires zero volts and is normally ground. (The tolerance and current requirements of the VDG are specified in the *DC Characteristics* table.)

Video Outputs (ϕA, ϕB, Y, CHB)
These four analog outputs are used to transfer luminance and color information to a standard NTSC color television receiver, either via the rf modulator or directly into Y, ϕA, and ϕB television video inputs.

Luminance (Y) – This six-level analog output contains composite sync, blanking, and four levels of video luminance.

ϕA – This three-level analog output is used in combination with the ϕB and Y outputs to specify one of eight colors.

ϕB – This four-level analog output is used in combination with the ϕA and Y outputs to specify one of eight colors. Additionally, one analog level is used to specify the time of the color burst reference signal.

Chroma Bias (CHB) – This pin is an analog output and provides a dc reference corresponding to the quiescent value of ϕA and ϕB. CHB is used to guarantee good thermal tracking and minimize the variation between the parts.

Synchronizing Inputs ($\overline{MS}$, CLK)

Three-State Control ($\overline{MS}$) – This is a TTL-compatible input that, when LOW, forces the VDG address lines into a high-impedance state. This may be done to allow other devices (such as an MPU) to address the display memory RAM.

Clock (CLK) – The VDG clock input (CLK) requires a 3.579545 MHz (standard) TV crystal frequency square wave. The duty cycle of this clock must be between 45 and 55 percent since it controls the width of alternate dots on the television screen.

Synchronizing Outputs ($\overline{FS}$, $\overline{HS}$, $\overline{RP}$)
Three TTL-compatible outputs provide circuits exterior to the VDG with timing references to the following internal VDG states:

Field Sync ($\overline{FS}$) – The HIGH-to-LOW transition of the $\overline{FS}$ output coincides with the end of active display area. During this time interval, an MPU may have total access to the display RAM without causing undesired flicker on the screen. The LOW-to-HIGH transition of $\overline{FS}$ coincides with the trailing edge of the vertical synchronization pulse.

Horizontal Sync ($\overline{HS}$) – The HIGH-to-LOW transition of the $\overline{HS}$ output coincides with the leading edge of the horizontal snyc pulse portion of the VDG luminance (Y) output.

Row Preset ($\overline{RP}$) – If desired, an external character generator ROM may be used with the VDG. In this configuration, an external 4-bit counter, used to supply row selection, is clocked by $\overline{HS}$ and cleared by the $\overline{RP}$ signal.

Mode Control Inputs ($\overline{A}$/G, $\overline{A}$/S, $\overline{INT}$/EXT, GM_0, GM_1, GM_2, CSS, INV)
Eight TTL-compatible inputs are used to control the operating mode of the VDG. $\overline{A}$/S, $\overline{INT}$/EXT, CSS and INV may be changed on a character-by-character basis. The CSS pin is used to select between two possible alphanumeric colors when the VDG is in the alphanumeric mode and between two color sets when the VDG is in the semigraphics-6 and full graphic mode. *Table 1* illustrates the various modes that can be obtained using the mode contol lines.

Display Modes

The VDG is capable of generating 12 distinct display modes. The color set selection (CSS) and invert (INV) pins allow variations on certain modes. The VDG displays two alphanumeric modes with two compatible semigraphic modes or one of eight full graphic modes. A detailed description of the various modes of operation follows. A summary of major modes can be found in *Table 2*, and a detailed description of VDG modes can be found in *Table 3*.

Alphanumeric Display Modes
All alphanumeric modes occupy an 8 x 12 dot character matrix box; there are 32 x 16 character boxes per TV frame. Each horizontal dot (dot-clock) corresponds to one-half the period duration of the 3.58 MHz clock, and each vertical dot is one scan line. One of two colors for the lighted dots may be selected by the color set select pin.

Internal Alphanumeric Mode – In the internal alphanumeric mode, an internal ROM will generate 64 ASCII display characters in a standard 5 x 7 box. Six bits of the 8-bit data word are used for the ASCII character generator; the two bits not used can be used to implement inverse video or color switching on a character-by-character basis. A 512-word display memory is required for this class of display.

External Alphanumeric Mode – In the external alphanumeric mode, an external character generator may be used to generate custom character sets of up to 256 separate 8 x 12 dot characters, each defined by an 8-bit data word. If fewer than eight bits are used for character definition, the remaining bits may be used for inverse video selection or color switching on a character-by-character basis. This display mode also requires a 512-word display memory.

Alpha Semigraphic-4 Mode – The alpha semigraphic-4 mode translates bits 0 through 3 into a 4 x 6 dot element in the standard 8 x 12 dot box. Three data bits may be used to select one of eight colors for the entire character box. The extra bit is available to implement mode switching on-the-fly. A 512-word display memory is required. A density of 64 x 32 elements is available in the display area. The element area is four dot-clocks wide by six lines high.

Alpha Semigraphic-6 Mode – The alpha semigraphic-6 mode maps six 4 x 4 dot elements into the standard 8 x 12 dot alphanumeric box, providing a screen density of 64 x 48 elements. Six bits are used to generate this map and two data bits may be used to select one of four colors in the display box. The element area is four dot-clocks wide by four lines high.

Full Graphic Mode

There are eight full graphic modes available from the VDG. These modes require 1K to 6K bytes of memory. The eight full graphic modes include an outside color border in one of two colors, depending upon the color set select (CSS) pin. The CSS pin selects one of two sets of four colors in the four color graphic modes.

The 64 x 64 Color Graphics Mode (Graphics One C) – The 64 x 64 color graphics mode generates a display matrix 64 elements wide by 64 elements high. Each element may be one of four colors. A 1K x 8 display memory is required. Each pictel equals four dot-clocks by three scan lines.

The 128 x 64 Graphics Mode (Graphics One R) – The 128 x 64 graphics mode generates a matrix 128 elements wide by 64 elements high. Each element may be either On or Off. However, the entire display may be one of two colors, selected by using the color set select pin. A 1K x 8 display memory is required. Each pictel equals two dot-clocks by three scan lines.

The 128 x 64 Color Graphics Mode (Graphics Two C) – The 128 x 64 color graphics mode generates a display matrix 128 elements wide by 64 elements high. Each element may be one of four colors. A 2K x 8 display memory is required. Each pictel equals two dot-clocks by three scan lines.

The 128 x 96 Graphics Mode (Graphics Two R) – The 128 x 96 graphics mode generates a display matrix 128 elements wide by 96 elements high. Each element may be either On or Off. However, the entire display may be one of two colors, selected by using the color set select pin. A 2K x 8 display memory is required. Each pictel equals two dot-clocks by two scan lines.

The 128 x 96 Color Graphics Mode (Graphics Three C) – The 128 x 96 color graphics mode generates a display 128 elements wide by 96 elements high. Each element may be one of four colors. A 3K x 8 display memory is required. Each pictel equals two dot-clocks by two scan lines.

The 128 x 192 Graphics Mode (Graphics Three R) – The 128 x 192 graphics mode generates a display matrix 128 elements wide by 192 elements high. Each element may be either On or Off, but the On elements may be one of two colors, selected with the color set select pin. A 3K x 8 display memory is required. Each pictel equals two dot-clocks by one scan line.

128 x 192 Color Graphics Mode (Graphics Six C) – The 128 x 192 color graphics mode generates a display 128 elements wide by 192 element high. Each element may be one of four colors. A 6K x 8 display memory is required. Each pictel equals two dot-clocks by one scan line.

The 256 x 192 Graphics Mode (Graphics Six R) – The 256 x 192 graphics mode generates a display 256 elements wide by 192 elements high. Each element may be either On or Off, but the On elements may be one of two colors, selected with the color set select pin. A 6K x 8 display memory is required. Each pictel equals one dot-clock by one scan line.

Table 1 Mode Control Inputs

$\overline{A/G}$	$\overline{A/S}$	$\overline{INT}$/EXT	INV	GM_2	GM_1	GM_0	Alpha/Graphic Mode Selected
0	0	0	0	X	X	X	Internal Alphanumeric
0	0	0	1	X	X	X	Internal Alphanumeric Inverted
0	0	1	0	X	X	X	External Alphanumeric
0	0	1	1	X	X	X	External Alphanumeric Inverted
0	1	0	X	X	X	X	Alpha Semigraphic-4
0	1	1	X	X	X	X	Alpha Semigraphic-6
1	X	X	X	0	0	0	64 x 64 Color Graphic
1	X	X	X	0	0	1	128 x 64 Graphic
1	X	X	X	0	1	0	128 x 64 Color Graphic
1	X	X	X	0	1	1	128 x 96 Graphic
1	X	X	X	1	0	0	128 x 96 Color Graphic
1	X	X	X	1	0	1	128 x 192 Graphic
1	X	X	X	1	1	0	128 x 192 Color Graphic
1	X	X	X	1	1	1	256 x 192 Graphic

Table 2 Summary of Major Modes

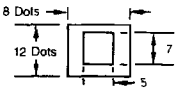
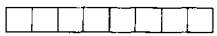
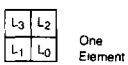
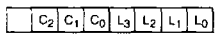
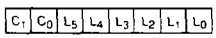
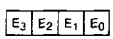
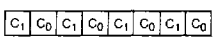
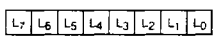
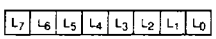
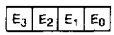
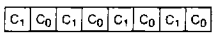
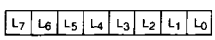
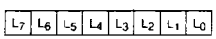
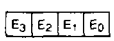
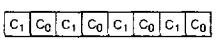
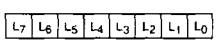
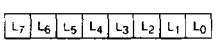
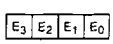
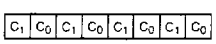
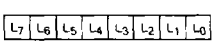
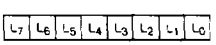
Title	Memory	Colors	Display Elements
Alphanumeric (Internal)	512 x 8	2	
Alphanumeric (External)	512 x 8	2	
Alpha Semigraphic-4	512 x 8	8	Box—Element
Alpha Semigraphic-6	512 x 8	4	Box—Element
64 x 64 Color Graphic	1K x 8	4	Matrix 64 x 64 Elements
128 x 64 Graphic*	1K x 8	2	Matrix 128 Elements Wide by 64 Elements High
128 x 64 Color Graphic	2K x 8	4	
128 x 96 Graphic*	1.5K x 8	2	Matrix 128 Elements Wide by 96 Elements High
128 x 96 Color Graphic	3K x 8	4	
128 x 192 Graphic*	3K x 8	2	Matrix 128 Elements Wide by 192 Elements High
128 x 192 Color Graphic	6K x 8	4	
256 x 192 Graphic*	6K x 8	2	Matrix 256 Elements Wide by 192 Elements High

*Graphic mode turns each element on or off. The color may be one of two.

Table 3 Detailed Description of VDG Modes

VDG Pins									Color		
$\overline{MS}$	$\overline{A/G}$	$\overline{A/S}$	$\overline{INT}/EXT$	GM_2	GM_1	GM_0	CSS	INV	Character Color	Background	Border
1	0	0	0	X	X	X	0	0	Green	Black	Black
								1	Black	Green	
							1	0	Orange	Black	Black
								1	Black	Orange	
1	0	0	1	X	X	X	0	0	Green	Black	Black
								1	Black	Green	
							1	0	Orange	Black	Black
								1	Black	Orange	
1	0	1	0	X	X	X	X	X	L_x C_2 C_1 C_0 Color 0 X X X Black 1 0 0 0 Green 1 0 0 1 Yellow 1 0 1 0 Blue 1 0 1 1 Red 1 1 0 0 Buff 1 1 0 1 Cyan 1 1 1 0 Magenta 1 1 1 1 Orange		Black
1	0	1	1	X	X	X	0	X	L_x C_1 C_0 Color 0 X X Black 1 0 0 Green 1 0 1 Yellow 1 1 0 Blue 1 1 1 Red 0 X X Black 1 0 0 Buff 1 0 1 Cyan 1 1 0 Magenta 1 1 1 Orange		Black
							1				
1	1	X	X	0	0	0	0	X	C_1 C_0 Color 0 0 Green 0 1 Yellow 1 0 Blue 1 1 Red 0 0 Buff 0 1 Cyan 1 0 Magenta 1 1 Orange		Green
							1				Buff
1	1	X	X	0	0	1	0	X	L_x 0 Color Black 1 Color Green		Green
							1		0 Black 1 Buff		Buff
1	1	X	X	0	1	0	0	X	Same Color as Graphics One C		Green
							1				Buff
1	1	X	X	0	1	1	0	X	Same Color as Graphics One R		Green
							1				Buff
1	1	X	X	1	0	0	0	X	Same Color as Graphics One C		Green
							1				Buff
1	1	X	X	1	0	1	0	X	Same Color as Graphics One R		Green
							1				Buff
1	1	X	X	1	1	0	0	X	Same Color as Graphics One C		Green
							1				Buff
1	1	X	X	1	1	1	0	X	Same Color as Graphics One R		Green
							1				Buff

Table 3 Detailed Description of VDG Modes (Cont.)

TV Screen		VDG Data Bus	Comments
Display Mode	**Detail**		
32 Characters in Columns 16 Characters in Rows			The internal alphanumeric mode uses an internal character generator that contains the following five dot by seven dot characters @ ABCDEF GHIJKLMNOPQRSTUVWXYZ [ ] ↑ ← SP !"#$%&'()*+,-./0123456789 ;<=>? The 6-bit ASCII code leaves two bits free; these may be externally connected to the mode pins ($\overline{A/G}$, $\overline{A/S}$, $\overline{INT}$/EXT, GM_2, GM_1, GM_0, CSS or INV)
32 Characters in Columns 16 Characters in Rows			The external alphanumeric mode uses an external character generator as well as a row counter Thus, custom character fonts are graphic symbol sets with up to 256 different 8 dot X 12 dot "characters" that may be displayed
64 Display Elements in Columns 32 Display Elements in Rows			The semigraphic-4 mode uses an internal "coarse graphics" generator in which a rectangle (8 dots by 12 dots) is divided into four equal parts The luminance of each part is determined by a corresponding bit on the VDG data bus The color of illuminated parts is determined by three bits
64 Display Elements in Columns 48 Display Elements in Rows			The semigraphic-6 mode is similar to the semigraphic-4 mode with the following differences The 8 dot by 12 dot rectangle is divided into six equal parts Color is determined by the two remaining bits
64 Display Elements in Columns 64 Display Elements in Rows			The graphics one C mode uses a maximum of 1024 bytes of display RAM in which one pair of bits specifies one picture element.
128 Display Elements in Columns 64 Display Elements in Rows			The graphics one R mode uses a maximum of 1024 bytes of display RAM in which one bit specifies one picture element
128 Display Elements in Columns 64 Display Elements in Rows			The graphics two C mode uses a maximum of 2048 bytes of display RAM in which one pair of bit specifies one picture element.
128 Display Elements in Columns 96 Display Elements in Rows			The graphics two R mode uses a maximum of 1536 bytes of display RAM in which one bit specifies one picture element.
128 Display Elements in Columns 96 Display Elements in Rows			The graphics three C mode uses a maximum of 3072 bytes of display RAM in which one pair of bytes specifies one picture element
128 Display Elements in Columns 192 Display Elements in Rows			The graphics three R mode uses a maximum of 3072 bytes of display RAM in which one bit specifies on picture element
128 Display Elements in Columns 192 Display Elements in Rows			The graphics six C mode uses a maximum of 6144 bytes of display RAM in which one pair of bit specifies one picture element.
256 Display Elements in Columns 192 Display Elements in Rows			The graphics six R mode uses a maximum of 6144 bytes of display RAM in which one bit specifies one picture element

5

Absolute Maximum Ratings

Supply Voltage, V_{CC}	−0.3 V, +7.0 V
Input Voltage, any Pin, V_{IN}	−0.3 V, +7.0 V
Operating Temperature Range, T_A	0°C, +70°C
Storage Temperature Range, T_{STG}	−65°C, +150°C
Power Dissipation, P_D	945 mW

Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device under these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics V_{CC} = 5.0 V ±5%, V_{SS} = 0.0 V, T_A = 0°C to +70°C, unless otherwise noted

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions
V_{IH}	Input HIGH Voltage CLK Other Inputs	 V_{SS} + 2.4 V_{SS} + 2.0		 V_{CC} V_{CC}	Vdc	
V_{IL}	Input LOW Voltage CLK Other Inputs	 V_{SS} − 0.3 V_{SS} − 0.3		 V_{SS} + 0.4 V_{SS} + 0.8	Vdc	
I_{in}	Input Leakage Current CLK, GM_0-GM_2, INV, $\overline{INT}$/EXT, $\overline{MS}$, V_{SS}, DD_0-DD_7, $\overline{A}$/S, $\overline{A}$/G			2.5	μAdc	
I_{LO}	Three-State (OFF State) Input Current DA_0-DA_{12}			10	μAdc	
V_{OH}	Output HIGH Voltage $\overline{RP}$, $\overline{HS}$, $\overline{FS}$	2.4			Vdc	C_{Load} = 30 pF I_{Load} = −100 μA
V_{OH}	Output HIGH Voltage DA_0-DA_{12}	2.4			Vdc	C_{Load} = 55 pF I_{Load} = −100 μA
V_{OL}	Output LOW Voltage $\overline{RP}$, $\overline{HS}$, $\overline{FS}$,			V_{SS} + 0.4	Vdc	C_{Load} = 30 pF I_{Load} = 1.6 mA
V_{OL}	Output LOW Voltage DA_0-DA_{12}			V_{SS} + 0.4	Vdc	C_{Load} = 55 pF I_{Load} = 1.6 mA
I_{OH}	Output HIGH Current (Sourcing) All Outputs (Except ϕA, ϕB, Y, and CHB)	−100			μAdc	V_{OH} = 2.4V
I_{OL}	Output LOW Current (Sinking) All Outputs (Except ϕA, ϕB, Y, and CHB	1.6			mAdc	V_{OL} = 0.4 Vdc
C_{IN}	Input Capacitance All Inputs			7.5	pF	V_{IN} = 0 T_A = 25°C f = 1.0 MHz
V_R	Chroma Bias Voltage		0.3 V_{CC}		Vdc	C_{Load} = 20 pF R_{Load} = 200 kΩ V_{CC} = 4.75 − 5.25 V
I_{CC}	Supply Current		90	114	mAdc	

DC Characteristics (Cont.)

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions
$V_{C\phi A}$	Chroma ϕA Voltage					
	V_{HI}		$V_R + 0.1\ V_{CC}$		Vdc	C_{Load} = 20 pF
	V_O		V_R			R_{Load} = 200 kΩ
	V_{LO}		$V_R - 0.1\ V_{CC}$			See *Figure 2*
$V_{C\phi B}$	Chroma ϕB Voltage					
	V_O		$V_R + 0.1\ V_{CC}$		Vdc	C_{Load} = 20 pF
	V_{Burst}		V_R			R_{Load} = 200 kΩ
	V_{LO}		$V_R - 0.05\ V_{CC}$			See *Figure 2*
			$V_R - 0.1\ V_{CC}$			
V_Y	Luminance Y Voltage					
	V_S		0.2 V_{CC}		Vdc	C_{Load} = 20 pF
	V_{BLANK}		0.75 V_S			R_{Load} = 200 kΩ
	V_{BLACK}		0.7 V_S			See *Figure 2*
V_{WL}	Voltage White Low		0.62			
V_{WM}	Voltage White Medium		0.5 V_S		Vdc	See *Figure 2*
V_{WH}	Voltage White High		0.38 V_S			

AC Characteristics V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C

Symbol	Characteristic	Min	Typ	Max	Unit	Conditions
f	CLK Frequency	3.579535	3.579545	3.579555	MHz	
CLK_{dc}	CLK Duty Cycle	45%	50%	55%		
	Chroma Phase Delay (Measured with Respect to Y Output)					See *Figure 3C*
t_{YA}	ϕA		200		ns	
t_{YB}	ϕB		200		ns	
t_{ry}	Luminance Rise Time		60		ns	See *Figure 3D*
t_{fy}	Luminance Fall Time		50		ns	
	Chroma Rise and Fall Times					
$t_rC\phi A$	ϕA Rise Time		60		ns	
$t_fC\phi A$	ϕA Fall Time		60		ns	See *Figure 3D*
$t_rC\phi B$	ϕB Rise Time		60		ns	
$t_fC\phi B$	ϕB Fall Time		60		ns	
t_{WFS}	Field Sync ($\overline{FS}$) Pulse Width		2.03		ms	See *Figure 3A*
	Row Preset ($\overline{RP}$)					
t_{WRP}	Pulse Width		0.98		μs	See *Figure 3B*
t_{HSRP}	Delay from $\overline{HS}$		0.98		μs	
t_{WHS}	Horizontal Sync ($\overline{HS}$)		4.9		μs	See *Figure 3B*

5

Fig. 2 Video and Chrominance Relationships Output Waveform

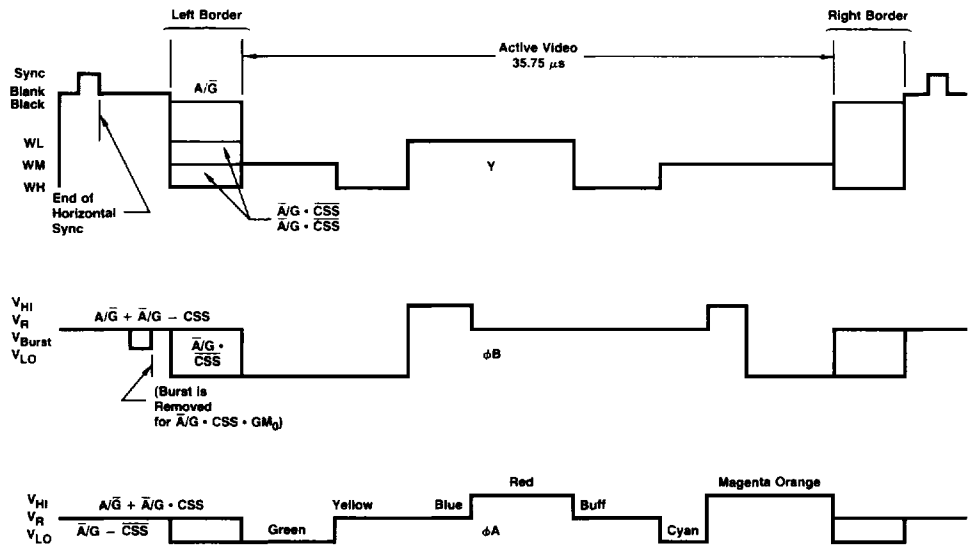
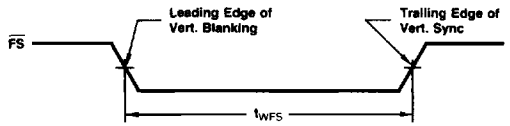
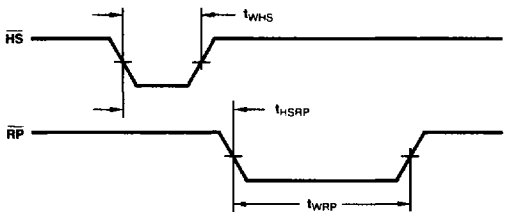


Fig. 3 Timing Diagrams

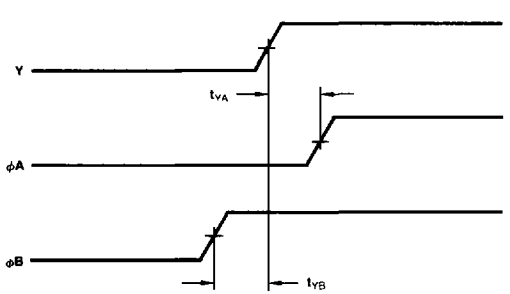
a. Field Sync



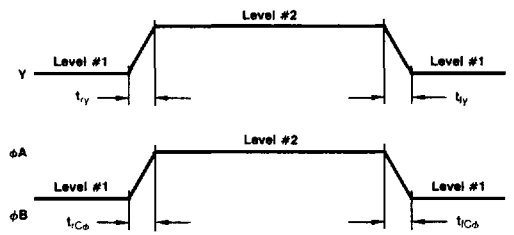
b. Row Preset



c. Chroma Phase Delay



d. Video and Fall Times



Ordering Information

Order Code	Temperature Range
F6847P, S	0°C to +70°C

P = Plastic Package
S = Ceramic Package