MOTOROLA
SEMICONDUCTORS
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC6847T1

Advance Information

MOS

(N-CHANNEL, SILICON-GATE)

NON-INTERLACE
VIDEO DISPLAY
GENERATOR

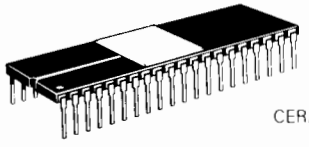
VIDEO DISPLAY GENERATOR

The video display generator (VDG) interfaces the M6800 microprocessor Family (or similar products) to a standard color NTSC television receiver. Applications of the VDG include video games, process control displays, home computers, education, communications, and graphics.

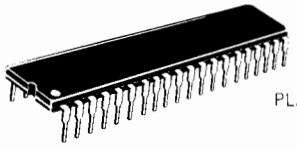
The VDG reads data from memory and produces a video signal which will allow the generation of alphanumeric or graphic displays. The generated video signal may be modulated to either channel 3 or 4 by using the compatible MC1372 (TV chroma and video modulator). This modulated signal is suitable for reception by a standard unmodified television receiver. A typical system block diagram is shown in Figure 2.

The MC6847T1 is an enhanced version of the MC6847 non-interlaced VDG. This device will only work with the SN74LS783 (MC6883) or SN74LS785 synchronous address multiplexer (SAM). Since all but the least significant address line (DA0) have been replaced by an 8-bit I/O port with enables and other signals, the need for external glue circuitry in the system design is reduced.

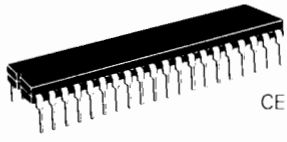
- Compatible with the M6800 and the M68000 Families, and Other Microprocessor Families
- Generates Four Different Alphanumeric Display Modes, One Semigraphic Mode, and Eight Graphic Display Modes
- The Alphanumeric Modes Display 32 Characters per Line by 16 Lines Using Either the Internal ROM or an External Character Generator
- Alphanumeric and Semigraphic Modes May Be Mixed on a Character-by-Character Basis
- Alphanumeric Modes Support Selectable Inverse on a Character-by-Character Basis or Lower Case on a Character-by-Character Basis
- Full Graphic Modes Offer Densities of 64 × 64, 128 × 64, 128 × 96, 128 × 192, or 256 × 192 Elements per Screen
- Full Graphic Modes Use One of Two Four-Color Sets or One of Two Two-Color Sets
- Compatible with the MC1372 and MC1373 Modulators via Y, R-Y (ϕA), and B-Y (ϕB) Interface
- Compatible with the SN74LS783 (MC6883) and SN74LS785 Synchronous Address Multiplexers
- Lowercase Has True Descenders for Ease of Reading



L SUFFIX
CERAMIC PACKAGE
CASE 715

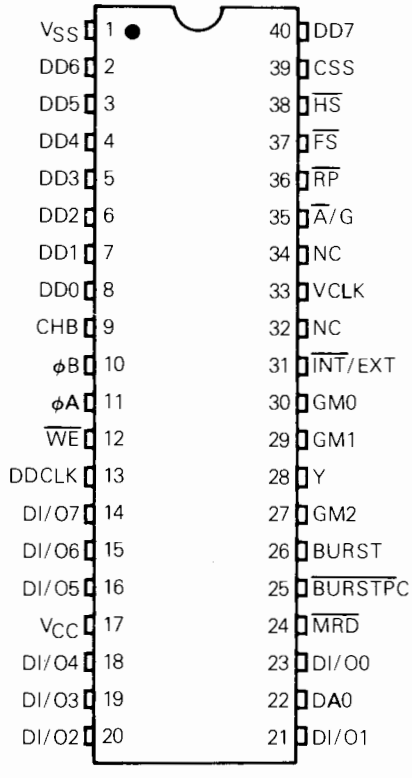


P SUFFIX
PLASTIC PACKAGE
CASE 711



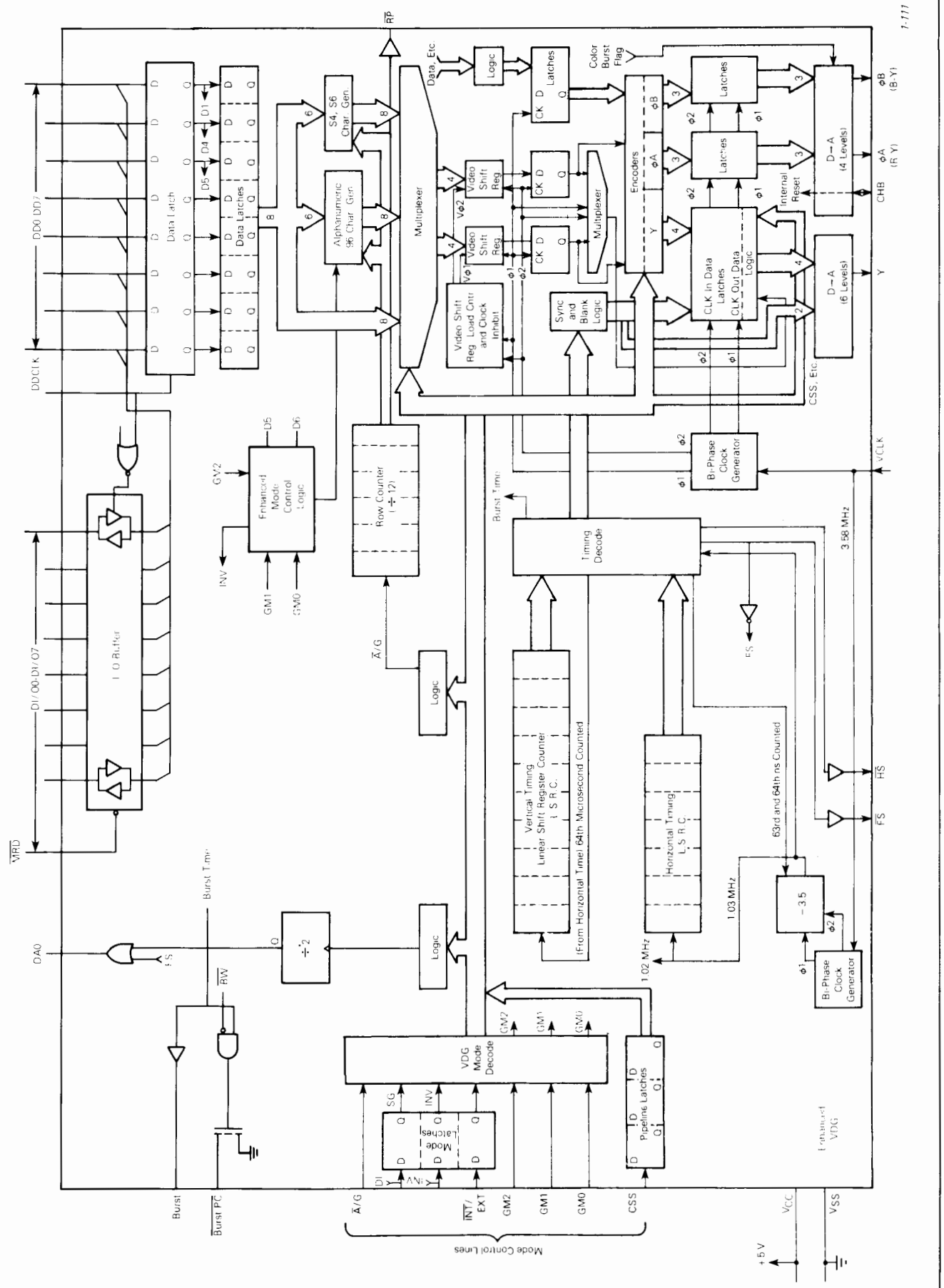
S SUFFIX
CERDIP PACKAGE
CASE 734

PIN ASSIGNMENT



This document contains information on a new product. Specifications and information herein are subject to change without notice.

FIGURE 1 – ENHANCED VDG BLOCK DIAGRAM



ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Characteristics	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	V
Input Voltage Any Pin	V_{in}	−0.3 to +7.0	V
Operating Temperature	T_A	0 to +70	°C
Storage Temperature	T_{stg}	−65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage (e.g., either V_{SS} or V_{CC}).

THERMAL CHARACTERISTICS

Characteristics	Symbol	Value	Unit
Thermal Resistance	θ_{JA}		°C/W
Ceramic		50	
Plastic		100	
Cerdip		60	

DC (STATIC) CHARACTERISTICS (V_{CC}=5.0 V±5%, V_{SS}=0.0 V, T_A=0°C to 70°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}				V
VCLK		V_{SS}+2.4	–	V_{CC}	
I/O Buffer Control ($\overline{WE}$, $\overline{MRD}$, DDCLK)		V_{SS}+3.0	–	V_{CC}	
I/O Port (DI/O0-DI/O7; DD0-DD7		V_{SS}+2.0	–	V_{CC}	
Other Inputs		V_{SS}+2.0	–	V_{CC}	
Input Low Voltage	V_{IL}				V
VCLK		V_{SS}−0.3	–	V_{SS}+4.0	
I/O Buffer Control ($\overline{WE}$, $\overline{MRD}$, DDCLK)		V_{SS}−0.3	–	V_{SS}+0.5	
I/O Port (DI/O0-DI/O7; DD0-DD7)		V_{SS}−0.3	–	V_{SS}+0.6	
Other Inputs		V_{SS}−0.3	–	V_{SS}+0.6	
Input Leakage Current (V_{in}=5.25 V) VCLK, GM0-GM2, INV, $\overline{INT}$/EXT, $\overline{A}$/G, DDCLK, $\overline{WE}$, $\overline{MRD}$, CSS	I_{in}	–	–	2.5	μA
Three-State (Off State) (V_{in}=0.4 to 2.4 V) DD0-DD7, DI/O0-DI/O7	I_{OL}	–	–	±10	μA
Output High Voltage (I_{Load}=−100 μA) DD7-DD0, DI/O7-DI/O0, $\overline{HS}$, $\overline{RP}$, FS, DA0, BURST	V_{OH}	2.4	–	–	V
Output Low Voltage (I_{Load}=1.6 μA) DD7-DD0, DI/O7-DI/O0, $\overline{HS}$, $\overline{RP}$, $\overline{FS}$, DA0, BURST, $\overline{BURSTPC}$	V_{OL}	–	–	V_{SS}+0.4	V
Input Capacitance (V_{in}=0, T_A=25°C, f=1.0 MHz) All Inputs	C_{in}	–	–	7.5	pF
Internal Power Dissipation (Measured at T_A=0°C to 70°C)	P_{INT}	–	–	600	mW
Chroma φA Voltage (see Figure 3)	V_{IH}	1.8	2.0	2.2	V
(C_{Load}=20 pF, R_{Load}=100 kΩ)	V_R	1.34	1.5	1.66	
(see Note)	V_{OL}	0.8	1.0	1.2	
Chroma φB Voltage (see Figure 3)	V_{IH}	1.8	2.0	2.2	V
(C_{Load}=20 pF, R_{Load}=100 kΩ)	V_R	1.34	1.5	1.66	
(see Note)	V_{OL}	0.8	1.0	1.2	
	V_{Burst}	1.07	1.25	1.43	

DC (STATIC) CHARACTERISTICS (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Luminance Y Voltage (see Figures 3 and 4) (C_{Load} = 20 pF, R_{Load} = 100 kΩ)					V
Voltage Synchronization	V_S	0.9	1.0	1.1	
Voltage Blank	V_{Blank}	0.63	0.77	0.9	
Voltage Black	V_{Black}	0.58	0.72	0.83	
Voltage White Low	V_{WL}	0.51	0.65	0.75	
Voltage White Medium	V_{WM}	0.40	0.54	0.66	
Voltage White High (see Note)	V_{WH}	0.27	0.42	0.53	
Chroma Bias Voltage (C_{Load} = 20 pF, R_{Load} = 100 kΩ)	V_R	0.27 V_{CC}	0.3 V_{CC}	0.33 V_{CC}	V
Resistor % of V_{SS} Tracking (Analog Outputs Linearity Error)	R_T	–	1.0	3.0	%

NOTE: The specified minimum and maximum numbers reflect performance of the VDG at the specified temperature range. Overlapping voltage levels will not occur. Refer to Figures 4 and 13.

FIGURE 2 — TYPICAL SYSTEM BLOCK DIAGRAM

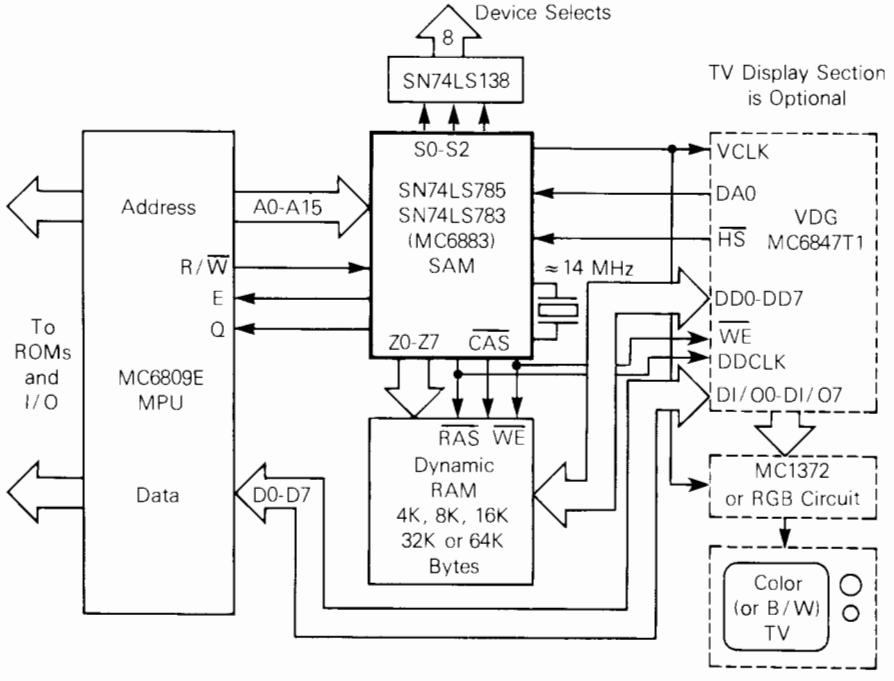
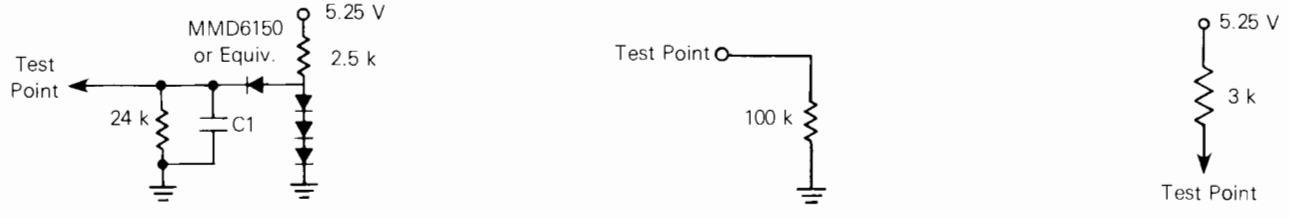


FIGURE 3 — TEST LOADS



A. DD0-DD7, DI/O0-DI/O7, BURST, DA0, $\overline{FS}$, $\overline{HS}$, $\overline{RP}$, Loads

B. CHB, ϕA, ϕB, Y Loads

C. $\overline{BURSTPC}$ Load

C1 = 30 pF for DA0, $\overline{FS}$, $\overline{HS}$, $\overline{RP}$, BURST
130 pF for DD7-DD0, DI/O7-DI/O0

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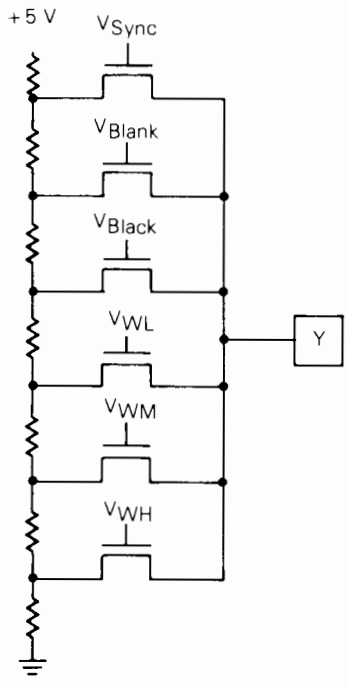
FIGURE 4 — PSEUDO ANALOG LUMINANCE RESISTOR CHAIN



NOTE: The chrominance output chain is similar in design to the luminance chain.

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POWER CONSIDERATIONS

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \bullet \theta_{JA}) \quad (1)$$

Where:

$T_A \equiv$ Ambient Temperature, °C

$\theta_{JA} \equiv$ Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D \equiv P_{INT} + P_{PORT}$

$P_{INT} \equiv I_{CC} \times V_{CC}$, Watts — Chip Internal Power

$P_{PORT} \equiv$ Port Power Dissipation, Watts — User Determined

For most applications $P_{PORT} \ll P_{INT}$ and can be neglected. P_{PORT} may become significant if the device is configured to drive Darlington bases or sink LED loads.

An approximate relationship between P_D and T_J (if P_{PORT} is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \bullet (T_A + 273°C) + \theta_{JA} \bullet P_D^2 \quad (3)$$

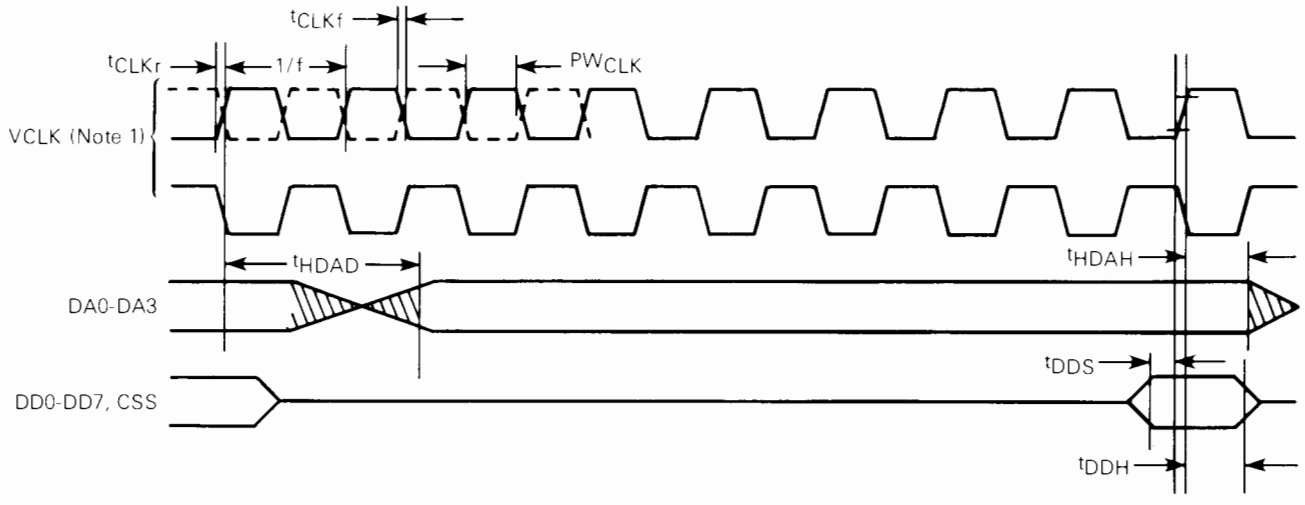
Where K is a constant pertaining to the particular part.

K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

AC (DYNAMIC) CHARACTERISTICS (V_{CC} = 5.0 V ±5%, T_A = 0°C to 70°C) (Load Circuit of Figure 3)

Characteristic		Symbol	Min	Max	Unit	Figure
CLK Frequency (3.579545 Color Burst Frequency)		f	3.579535	3.597555	MHz	5
CLK Duty Cycle		CLK_{dc}	45	55	%	5
Clock Rise Time		t_{CLKr}	–	50	ns	5
Clock Fall Time		t_{CLKf}	–	50	ns	5
Clock Pulse Width		PW_{CLK}	120	160	ns	5
Horizontal Display Address Delay from Counter	DA0-DA3	t_{HDAD}	–	490	ns	5,6,10
	DA4	t_{HDA4D}	–	550	ns	5,6,10
Horizontal Display Address Hold Time		t_{HDAH}	0	–	ns	5,6,10
Display Data Setup Time	CSS, INV, $\overline{A}$/S, $\overline{INT}$/EXT, DD0-DD7	t_{DDS}	70	–	ns	5,6,10
Display Data Hold Time	CSS, INV, $\overline{A}$/S, $\overline{INT}$/EXT, DD0-DD7	t_{DDH}	140	–	ns	5,6,10
Horizontal Sync ($\overline{HS}$) Delay	Fall	t_{DHSf}	–	550	ns	11
	Rise	t_{DHSr}	–	740		
Row Preset ($\overline{RP}$) Delay	Fall	t_{DRPf}	–	660	ns	11
	Rise	t_{DRDr}	–	540		
Field Sync ($\overline{FS}$) Delay	Fall	t_{DFSf}	–	520	ns	12
	Rise	t_{DFSr}	–	600		
Chroma Rise and Fall Times					ns	14
(ϕA Rise Time)		$t_{rC\phi A}$	–	100		
		$t_{r\phi A}$	–	100		
(ϕA Fall Time)		$t_{fC\phi A}$	–	100		
		$t_{f\phi A}$	–	100		
(ϕB Rise Time)		$t_{rC\phi B}$	–	100		
		$t_{r\phi B}$	–	100		
(ϕB Fall Time)		$t_{fC\phi B}$	–	100		
		$t_{f\phi B}$	–	100		
Color Burst Rise Time on ϕB Output		t_{CBr}	–	100	ns	14
Color Burst Fall Time on ϕB Output		t_{CBf}	–	100	ns	14
Chroma Phase Delay (Measured with Respect to "Y" Output)					ns	
ϕA		t_{YA}	–50	140		19
ϕB		t_{YB}	–50	140		
Luminance Rise Time		t_{ry}	–	100	ns	14
Luminance Fall Time		t_{fy}	–	100	ns	14
Horizontal Sync Rise Time on Y Output		t_{Hr}	–	100	ns	14
Horizontal Sync Fall Time on Y Output		t_{Hf}	–	100	ns	14
Horizontal Blanking Rise Time on Y Output		t_{HBr}	–	100	ns	14
Horizontal Blanking Fall Time on Y Output		t_{HBf}	–	100	ns	14
Front Porch Duration Time (7 × 1/f)		t_{FP}	1.8	2.4	µs	14
Back Porch Duration Time (17.5 × 1/f)		t_{BP}	4.5	5.1	µs	14
Left Border Duration Time (29 × 1/f)		t_{LB}	7.5	8.3	µs	14
Right Border Duration Time (29 × 1/f)		t_{RB}	7.5	8.3	µs	14
Color Burst Duration Time (10.5 × 1/f)		t_{CB}	2.7	3.2	µs	14
Data Port Characteristics					ns	
Display Data Setup Before DDCLK		t_{su}	110	–		8
Propagation Delay, MPU Read		t_{prop}	125	–		9
Write Enable to Valid Output		t_{WEO}	125	–		9
DDCLK Rise to DA0 Time		t_{DVA}	–	280	ns	8
Mode Inputs Valid to DA0 Time		t_{MVA}	–	230	ns	8

FIGURE 5 — CLOCK AND LONG CYCLE HORIZONTAL ACCESS TIMING



NOTES:
1. The VDG may power-up using either the rising or falling edge of the clock (dotted line).
2. Long cycle timing applies to CG1, RG1, RG2, and RG3 modes (see Table 5). The $\overline{A}/G$ signal is high. The $\overline{INT}$/EXT and INV input levels do not affect the VDG in long cycle modes.
3. All timing is measured to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts unless otherwise specified.

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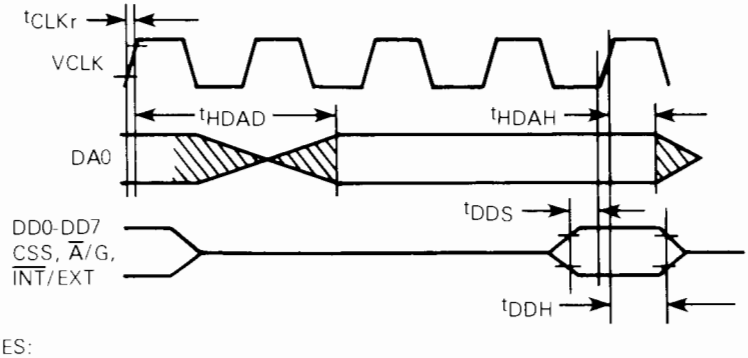
FIGURE 6 — SHORT CYCLE HORIZONTAL ACCESS TIMING



NOTES:
1. The VDG may power-up using either the rising or falling edge of the clock as shown in Figure 5.
2. Short cycle timing applies to the four alphanumeric modes, the semigraphic mode, and to the CG2, CG3, CG6, RG6 modes (see Table 5). For the four graphic modes, $\overline{A}/G$ is high and the $\overline{INT}$/EXT and INV levels do not affect the VDG.
3. All timing is measured to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts unless otherwise specified.

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FIGURE 7 — CHROMA PHASE DELAY

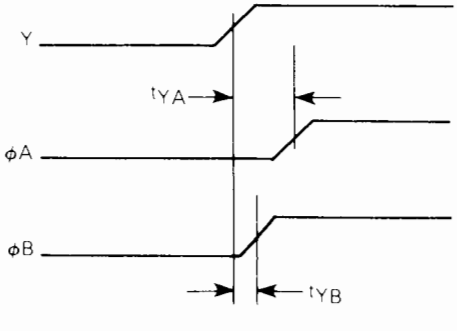

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FIGURE 8 — DISPLAY ACCESS TIMING

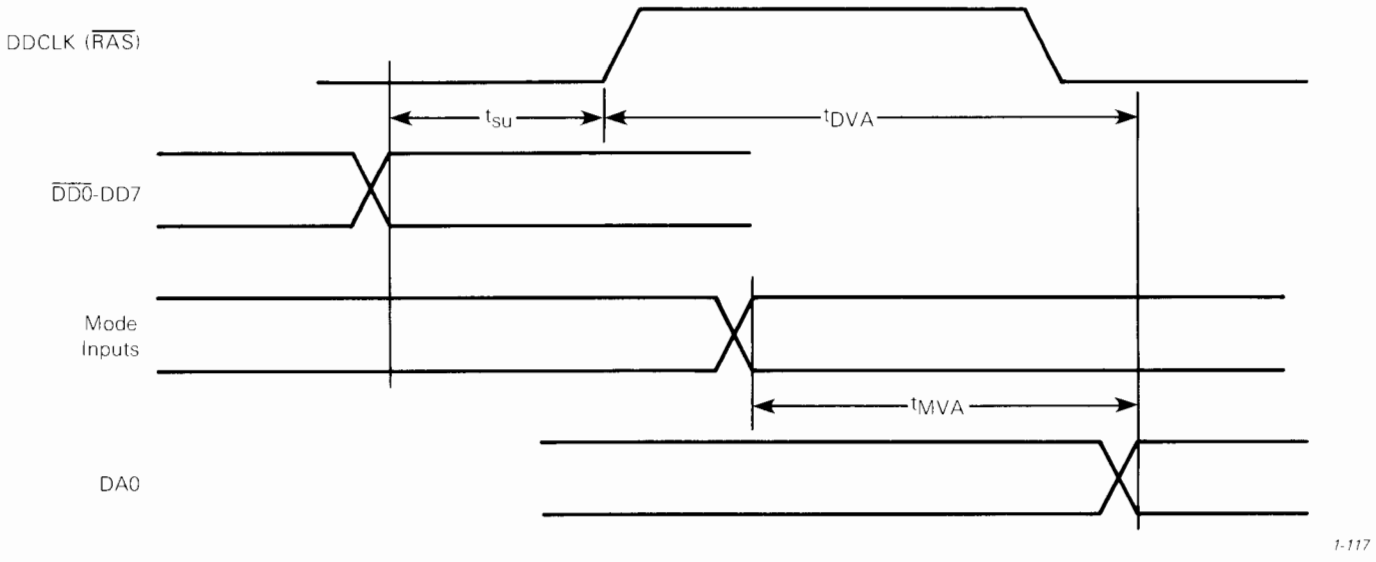


FIGURE 9 — DATA PORT TIMING

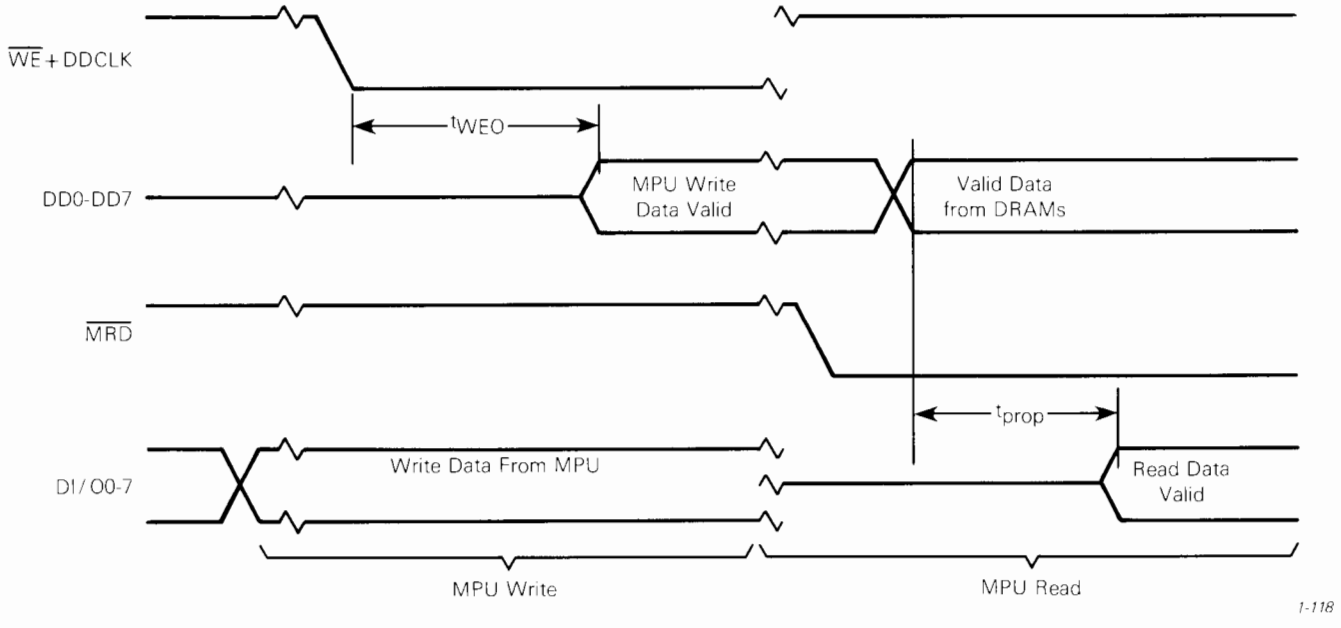
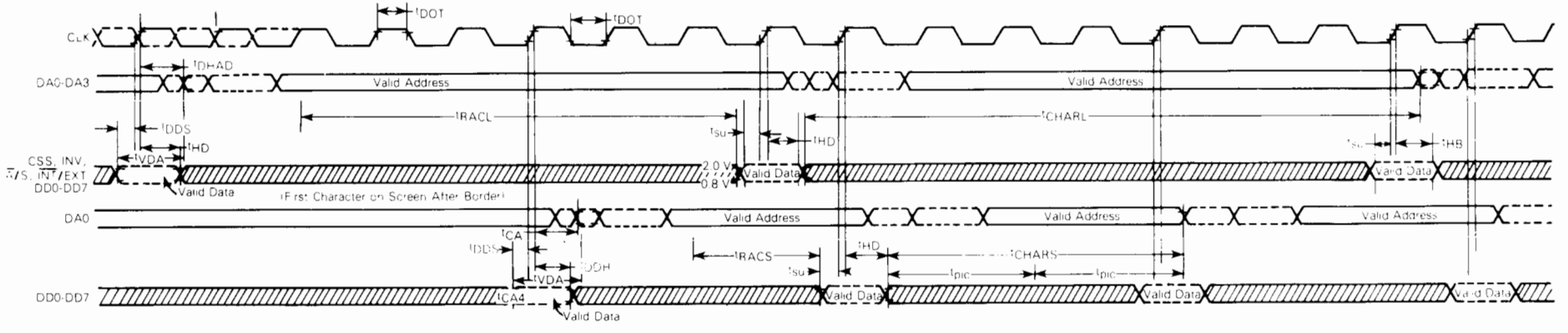


FIGURE 10 — HORIZONTAL ADDRESS AND VALID DATA SETUP AND HOLD TIMING



NOTE:

Timing relationships are shown from the beginning of the line.

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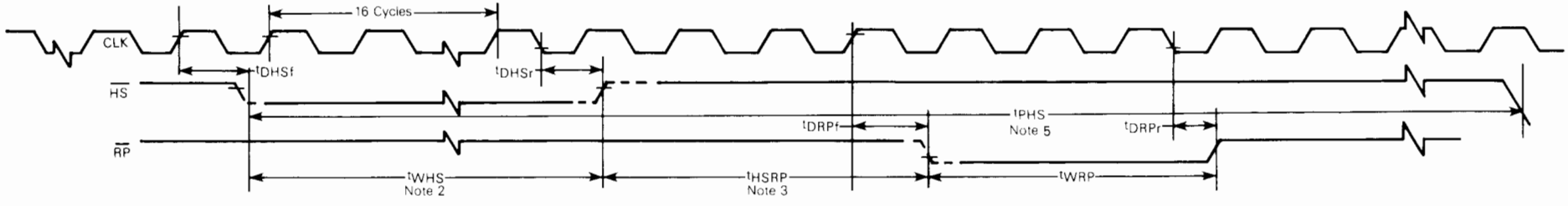
FIGURE 11 — VERTICAL ADDRESS, ROW PRESET, AND HORIZONTAL SYNCHRONIZATION TIMING



NOTES:

1. All timing is measured to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts unless otherwise specified.
2. $\overline{HS}$ pulse width may be determined by $t_{WHS} = 16.5 \cdot 1/f - t_{DHSF} + t_{DHSr}$.
3. $\overline{HS}$ to $\overline{RP}$ may be determined by $t_{HSRP} = 3.5 \cdot 1/f - t_{DHSr} + t_{DRPf}$.
4. $\overline{RP}$ pulse width may be determined by $t_{WRP} = 3.5 \cdot 1/f - t_{DRPf} + t_{DRPr}$.
5. $t_{PHS} = 228 \cdot 1/f$.
6. $t_{DOT} = 1/2\,f$.

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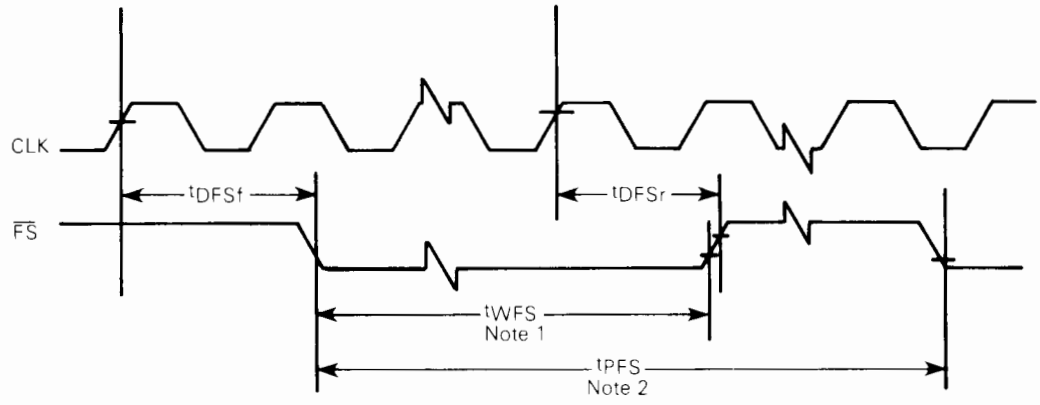
FIGURE 12 — FIELD SYNC ($\overline{FS}$) TIMING



NOTES:

1. $t_{WFS} = 32 \cdot t_{PHST} = 32 \cdot (228 \cdot 1/f)$
2. $t_{PFS} = 262 \cdot t_{PHST} = 262 = (228 \cdot 1/f)$

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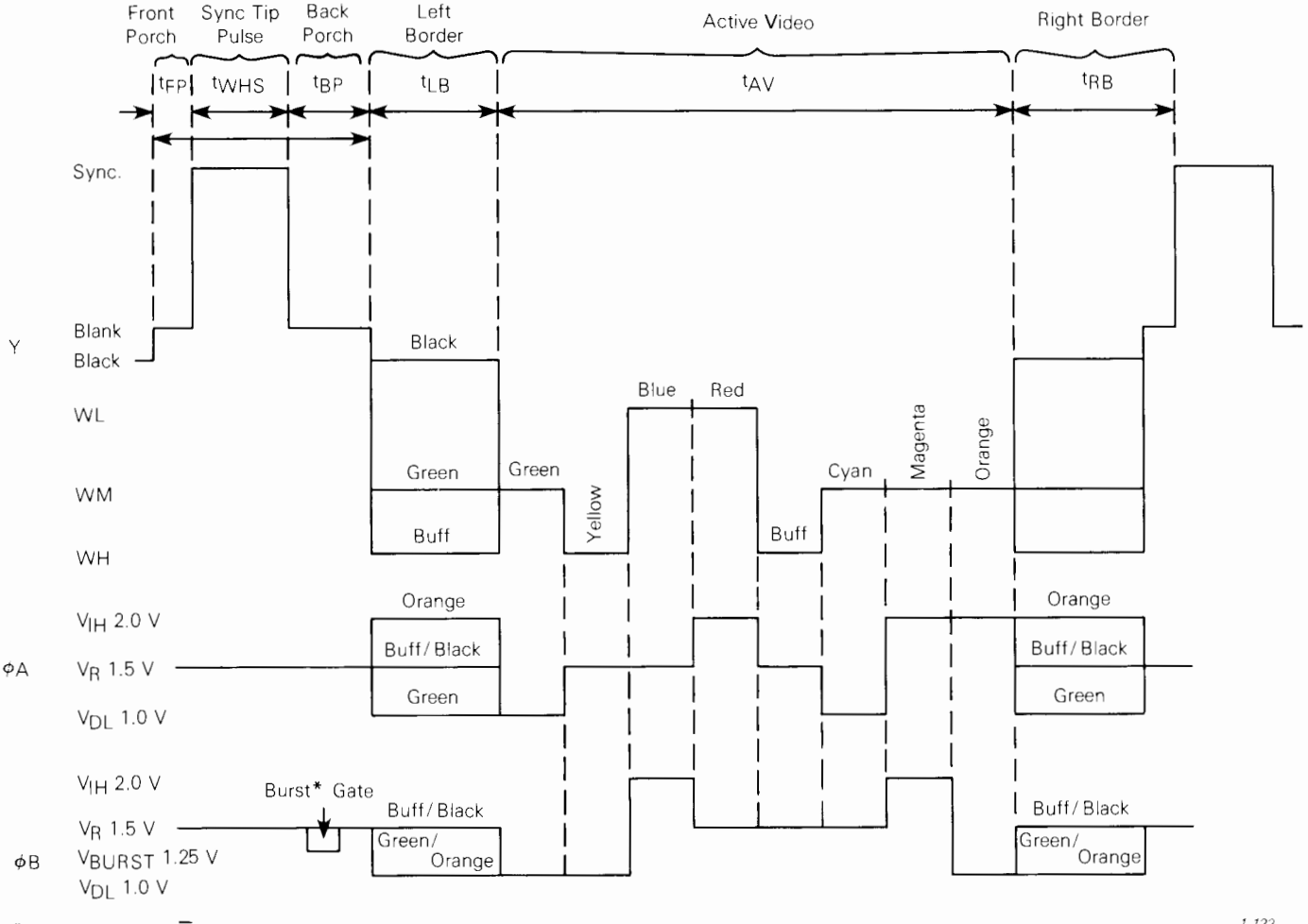
FIGURE 13 — VIDEO AND CHROMINANCE OUTPUT WAVEFORM RELATIONSHIPS



*No burst flag for $\overline{A}/G$, CSS, GM0

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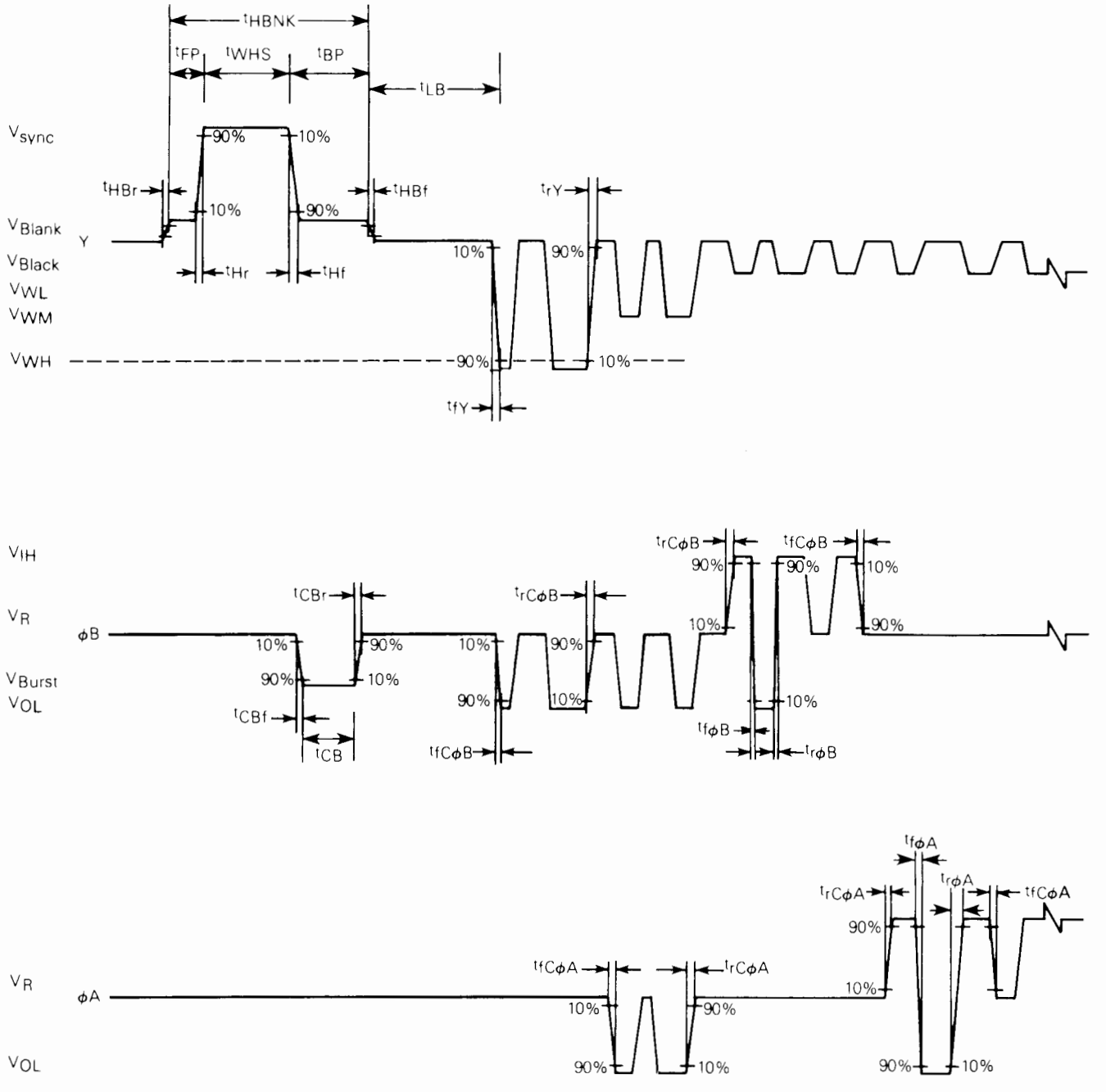
FIGURE 14 – VIDEO RISE AND FALL TIMING DIAGRAMS



NOTE: Illustrates beginning of one horizontal line.

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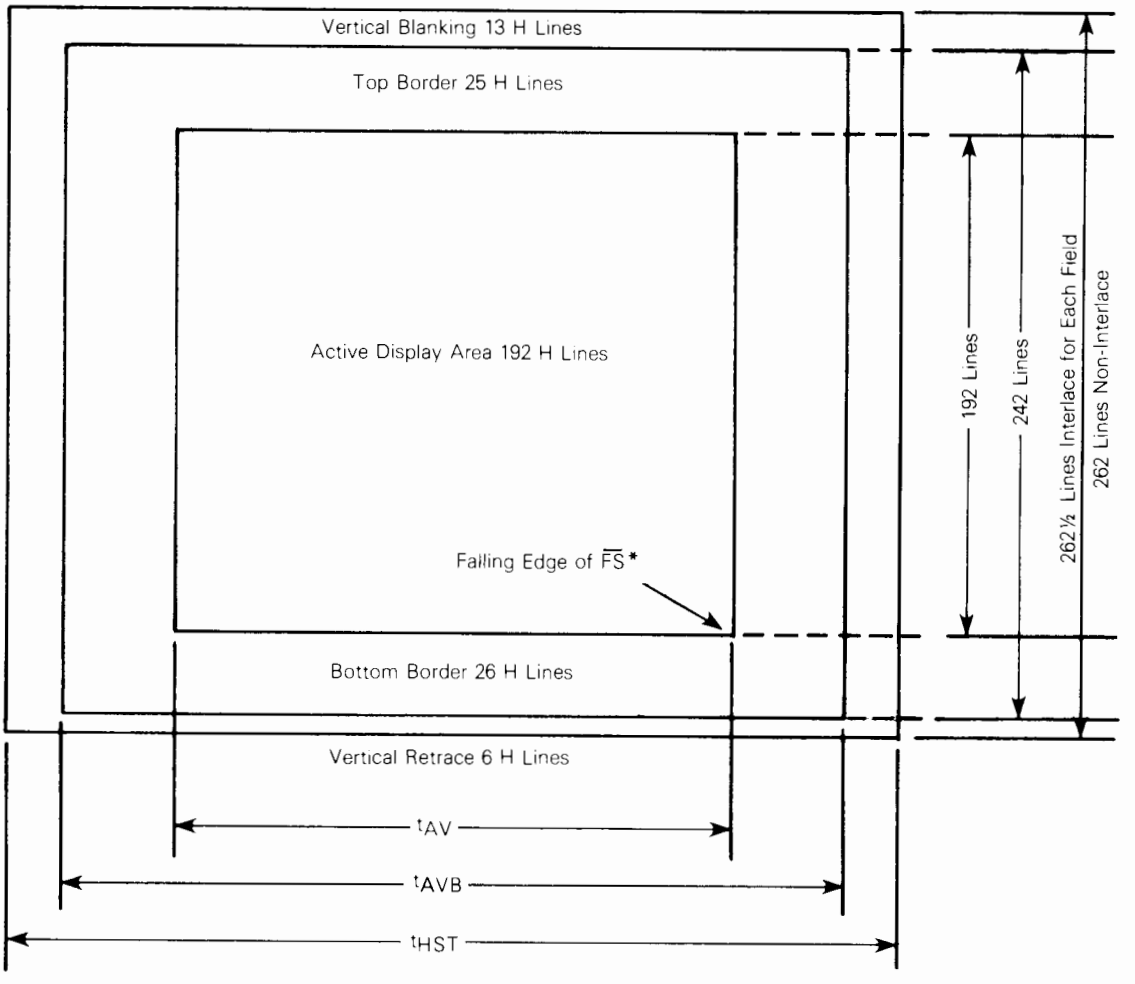
FIGURE 15 — DISPLAY AREA TIMING



* Typically 2.4 μs after start of vertical blank.

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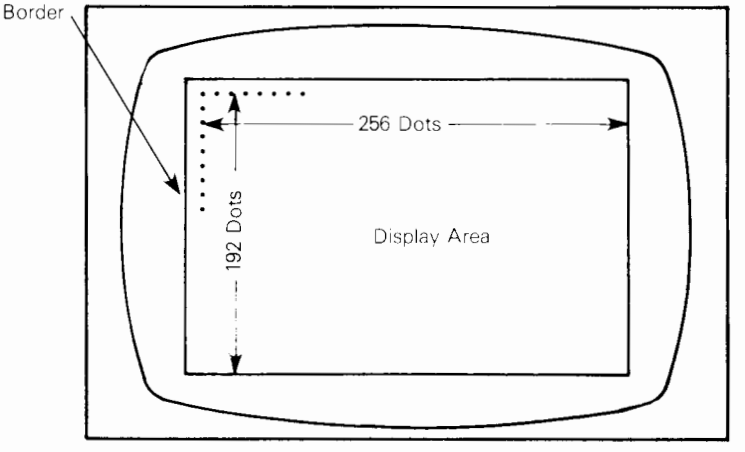
FIGURE 16 — TYPICAL FORMAT OF THE TELEVISION SCREEN



NOTE: The border is black, green, or orange in alpha/semigraphic modes and is green or buff (off-white) in all graphic modes. The border color is controlled by the VDG.

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GENERAL DESCRIPTION

The MC6847T1 video display generator (VDG) provides a simple interface for display of digital information on a color monitor or standard color/black-and-white television receivers.

Television transmissions in North and South America and Japan conform to the National Television System Committee (NTSC) standards. This system is based on a field repetition rate of 60 fields per second. There are 525 interlaced lines per frame or one-half this number per field.

The VDG scans one field of 262 lines 60 times per second. This non-interlace VDG is recommended for use in systems, i.e., TV games and personal computers, where absolute NTSC compatibility is not required.

NOTE

A system with the MC6847T1 VDG and the MC1372 video modulator forms a transmitter which transmits at 61.2 MHz (channel 3) or 67.25 MHz (channel 4) depending on component values chosen. Since this is a Class I TV device, care must be taken to meet FCC requirements Part 15, Subpart H. However if the composite video output from the MC1372 drives the television directly, Section 15.7 of the FCC specification must be adhered to.

SIGNAL DESCRIPTION

The signal descriptions are arranged alphabetically by function.

MPU/MEMORY INTERFACE SIGNALS

Data Address (DA0)

The DA0 signal is the only address line available in the VDG. It is not three-stated and is gated with the $\overline{FS}$ signal. Whenever $\overline{FS}$ is low, DA0 is high and whenever $\overline{FS}$ is high, DA0 functions normally.

When DA0 is high during the horizontal sync ($\overline{HS}$) transition from low to high, the SN74LS783/785 synchronous address multiplexer (SAM) is instructed to do a vertical preset to the vertical address counters from the F bits in the SAM control register. The DA0 signal toggles the address counters in the SAM on the high-to-low transition. The DA0 period is equal to two character times and allows the SAM to access 16 or 32 memory locations during active video time depending upon the display mode selected.

Data Display (DD0 through DD7)

These eight TTL-compatible data signals are used to input data from RAM to be processed by the VDG. The data is then interpreted and transformed into luminance (Y) and chroma outputs (ϕA and ϕB).

Bit 8 (DD7) is used to switch to the compatible semigraphic mode on a character-by-character basis. Bit seven (DD6) is used to select either an inverted upper case character or a lower case character. GM0 is used to determine if DD6 performs an invert or lower case function. If GM0 is high, then lower case is enabled. If GM0 is low, then DD6 is used to invert the display on a character-by-character basis. The remaining six bits select the character to be displayed (see Figure 17).

FIGURE 17 — FUNCTIONS OF DATA DISPLAY SIGNALS

DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
A/S	INV* or LC**	Character to Be Displayed					

*When GMO is zero, DD6 is invert (INV).
**When GMO is one, DD6 is lower case (LC).

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Display Data Clock (DDCLK)

The DDCLK (row address select, RAS) signal is used to latch the video display data into the VDG. It is normally connected to RAS from the SAM. Data is latched on the low-to-high transition. No external latches are needed.

Data I/O (DI/O0 through DI/O7)

These DI/O signals are used to form an 8-bit bidirectional port with the DD0 through DD7 signals. The port has three-state outputs and separate enables for each direction. These signals replace the SN74LS244 used in the MC6847 system. This does not allow the full double-speed mode of operation when writing to the DRAMs through the I/O port.

The full double-speed mode is possible in the 16K × 4 system if an external SN74LS244 is used instead of the VDG port. The external SN74LS244 is not needed when using the 16K × 1s or the 64K × 1s in double-speed mode because their data inputs can be connected directly to the MPU's data bus. See Figures 18 and 19.

MPU Read ($\overline{MRD}$)

The $\overline{MRD}$ signal is an active low enable to the 8-bit I/O port. It enables the three-state buffers which connect the DRAM data I/O signals to the MPU data bus when reading the DRAMs.

Write Enable ($\overline{WE}$)

The $\overline{WE}$ signal is used to generate one of the active low enables to the 8-bit I/O port. The $\overline{WE}$ signal is gated internally with DDCLK. It is used to enable the three-state buffers which connect the MPU data bus to the DRAM I/O signals when writing to the DRAMs. The $\overline{WE}$ signal is normally connected to the $\overline{WE}$ output of the SAM.

MODE CONTROL SIGNALS

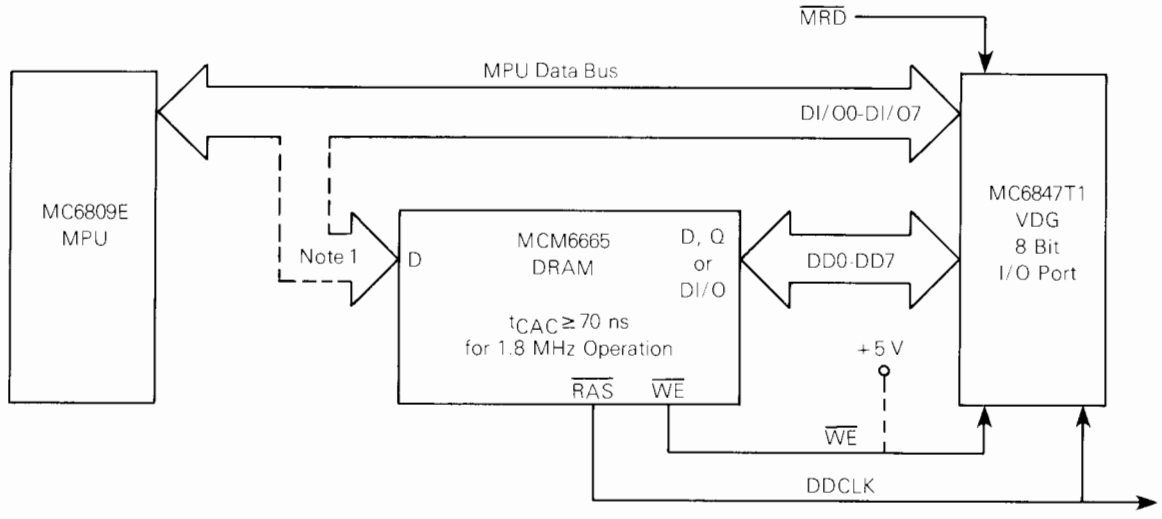
Alpha Graphic ($\overline{A}$/G)

This TTL-compatible input signal is used to control the operating mode of the VDG. When the $\overline{A}$/G signal is in the low or alpha position, the alphanumeric or semigraphic mode is selected. It is possible to display internal or external characters. In the external mode, the SN74LS161 must be parallel loaded with a different count than the VDG if the characters are to be on the same scan lines as the internal characters. This is necessary since the characters in the VDG have been moved up two scan lines to allow room for the descenders on the lowercase characters.

Color Set Select (CSS)

This TTL-compatible input signal is used to select between two possible alphanumeric colors when the VDG is in the alphanumeric mode and between two color sets when the VDG is in the full graphic modes. The CSS signal may be changed on a character-by-character basis.

FIGURE 18 — MPU WRITES IN DOUBLE-SPEED MODE USING 16K × 1 OR 64K × 1 DRAM



NOTES:
1. When connected, $\overline{WE}$ of the MC6847T1 VDG must be tied to a +5 V source.
2. This configuration is not possible with 16K × 4 DRAMs because they do not have a separate data input signal. See Figure 19.

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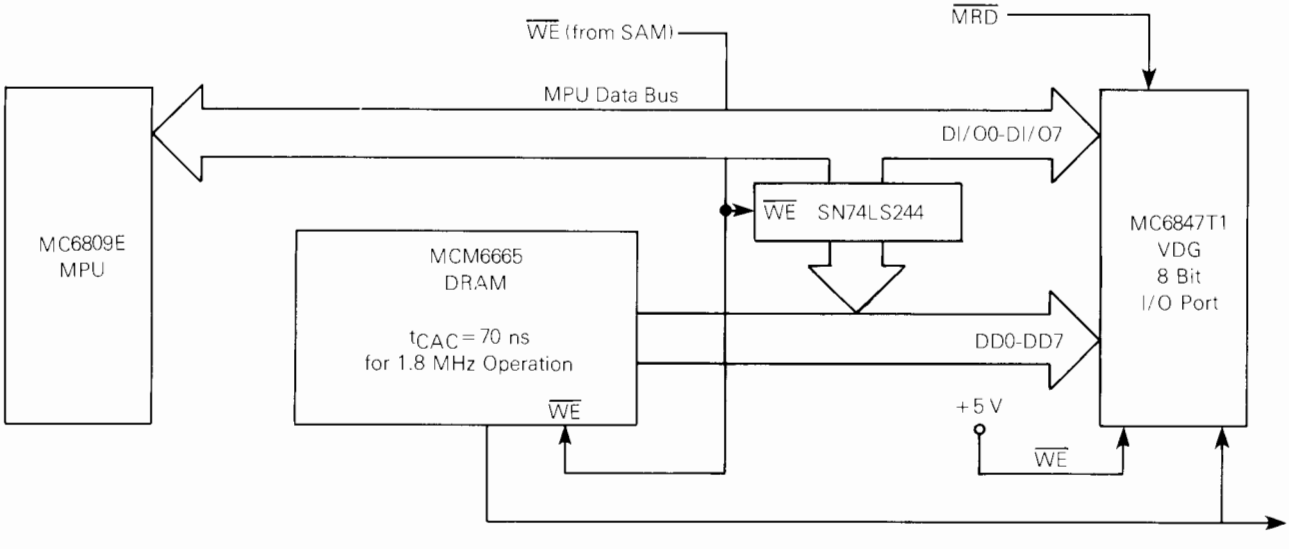
FIGURE 19 — MPU WRITES IN DOUBLE-SPEED MODE USING 64K × 4 DRAM



NOTE: SN74LS244 is used instead of the VDG write port to achieve 1.8 MHz operation.

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Graphic Mode (GM0 through GM2)

The GM0 signal must be high to enable the lower-case characters. When GM0 is low, DD6 performs the invert function. This eliminates the need for the invert signal.

The GM1 signal works as a screen invert signal in the alpha modes. When low, alpha modes 1 and 2 are enabled. When high, modes 3 and 4 are enabled. Mode 3 is the inverse of mode 1 and mode 4 is the inverse of mode 2. For a complete description of the enhanced alpha modes, see Table 2. The internal alpha mode has a character font of 96 characters including uppercase and lowercase and some symbols. A complete list of the characters is shown in Figure 20.

The GM2 signal works as a border color enhance enable signal. When low, the alpha border colors are always black. When high, the enhanced border colors are enabled and depend on CSS and GM1 (see Table 3).

Internal/External ($\overline{INT}$/EXT)

This TTL-compatible input is used to determine whether or not the VDG's internal character ROM is selected. It may be changed on a character-by-character basis. Table 1 illustrates the function of the mode control lines.

TABLE 1 — MODE CONTROL LINES (INPUTS)

$\overline{A}$/G	INT/EXT	GM2	GM1	GM0	D7	Alpha/Graphic Mode Select	Color Sets	Colors
0	0	Note 1	Note 1	X	1	Semigraphic 4	8	1
0	0	Note 1	0	0	0	Alpha Internal Mode 1 (Note 3)	Note 2	2
0	0	Note 1	0	1	0	Alpha Internal Mode 2 (Note 3)	Note 2	2
0	0	Note 1	1 Note 4	0	0	Alpha Internal Mode 3 (Note 3)	Note 2	2
0	0	Note 1	1 Note 4	1	0	Alpha Internal Mode 4 (Note 3)	Note 2	2
0	1	Note 1	X	X	1	Not Valid, Do Not Use	Note 2	X
0	1	Note 1	0	0	0	Alpha External Mode 1	Note 2	2
0	1	Note 1	0	1	0	Alpha External Mode 2	Note 2	2
0	1	Note 1	1 Note 4	0	0	Alpha External Mode 3	Note 2	2
0	1	Note 1	1 Note 4	1	0	Alpha External Mode 4	Note 2	2
1	X	0	0	0	D7	CG1 64 × 64	4	2
1	X	0	0	1	D7	RG1 128 × 64	2	2
1	X	0	1	0	D7	CG2 128 × 64	4	2
1	X	0	1	1	D7	RG2 128 × 96	2	2
1	X	1	0	0	D7	CG3 128 × 96	4	2
1	X	1	0	1	D7	RG3 128 × 192	2	2
1	X	1	1	0	D7	CG6 128 × 192	4	2
1	X	1	1	1	D7	RG6 256 × 192	2	2

NOTES:
1. Changes border color only.
2. Characters can be green, orange, or black.
3. See character font table (Figure 20).
4. Affects border color.

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TABLE 2 — ENHANCED ALPHA MODES FOR THE MC6847T1 VDG

CSS	Border Color	Alpha	GM1	GM0	DD7	DD6	DD5	Characters
0	Green	1	0	0	0	0	0	Noninverted Uppercase Alphabet
1	Orange				0	0	1	Noninverted Punctuation and Numbers
	(see Note 1)				0	1	0	Inverted Uppercase Alphabet
					0	1	1	Inverted Punctuation and Numbers
0	Green	2	0	1	0	0	0	Noninverted Uppercase Alphabet
1	Orange				0	0	1	Noninverted Punctuation and Numbers
	(see Note 1)				0	1	0	Inverted Uppercase Alphabet
					0	1	1	Inverted Punctuation and Numbers
0	Black	3	1	0	0	0	0	Noninverted Uppercase Alphabet
1	Black				0	0	1	Noninverted Punctuation and Numbers
					0	1	0	Inverted Uppercase Alphabet
					0	1	1	Inverted Punctuation and Numbers
0	Black	4	1	1	0	0	0	Noninverted Uppercase Alphabet
1	Black				0	0	1	Noninverted Punctuation and Numbers
					0	1	0	Inverted Uppercase Alphabet
					0	1	1	Inverted Punctuation and Numbers

Alphanumeric Character							
B7	B6	B5	B4	B3	B2	B1	B0
A/S	INV/LC	CC5	CC4	CC3	CC2	CC1	CC0

NOTES:
1. GM2 must be high to obtain these border colors. If GM2 is low, the border color is always black.
2. B6 can be either invert or lower case.
3. The display data requires 512 bytes.

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TABLE 3 — BORDER COLOR TRUTH TABLE

GM2	GM1	CSS	Border Color
0	X	X	Black
1	0	0	Green
1	0	1	Orange
1	1	0	Black
1	1	1	Black

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FIGURE 20 — ALPHA MODE CHARACTER TABLE

Alpha Mode D7=0*	GM1	GM0	D6	D5	DD0-DD4 in HEX
					00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F
1	0	0	0	0	@ A B C D E F G H I J K L M N O P Q R S T U V W X Y Z [\ ] ↑ ←
			0	1	SP ! " # $ % & ' ( ) * + , - . / 0 1 2 3 4 5 6 7 8 9 : ; < = > ?
			1	0	@ A B C D E F G H I J K L M N O P Q R S T U V W X Y Z [\ ] ↑ ←
			1	1	SP ! " # $ % & ' ( ) * + , - . / 0 1 2 3 4 5 6 7 8 9 : ; < = > ?
2	0	1	0	0	^ a b c d e f g h i j k l m n o p q r s t u v w x y z { | } ~ _
			0	1	SP ! " # $ % & ' ( ) * + , - . / 0 1 2 3 4 5 6 7 8 9 : ; < = > ?
			1	0	@ A B C D E F G H I J K L M N O P Q R S T U V W X Y Z [\ ] ↑ ←
			1	1	SP ! " # $ % & ' ( ) * + , - . / 0 1 2 3 4 5 6 7 8 9 : ; < = > ?
	1	0	0	0	@ A B C D E F G H I J K L M N O P Q R S T U V W X Y Z [\ ] ↑ ←
			0	1	SP ! " # $ % & ' ( ) * + , - . / 0 1 2 3 4 5 6 7 8 9 : ; < = > ?
			1	0	@ A B C D E F G H I J K L M N O P Q R S T U V W X Y Z [\ ] ↑ ←
			1	1	SP ! " # $ % & ' ( ) * + , - . / 0 1 2 3 4 5 6 7 8 9 : ; < = > ?
4	1	1	0	0	^ a b c d e f g h i j k l m n o p q r s t u v w x y z { | } ~ _
			0	1	SP ! " # $ % & ' ( ) * + , - . / 0 1 2 3 4 5 6 7 8 9 : ; < = > ?
			1	0	@ A B C D E F G H I J K L M N O P Q R S T U V W X Y Z [\ ] ↑ ←
			1	1	SP ! " # $ % & ' ( ) * + , - . / 0 1 2 3 4 5 6 7 8 9 : ; < = > ?

NOTES:

1. Black characters are noninverted. Possible colors are green and orange.
2. White characters are inverted. Possible background colors are green and orange.
3. D7 is internally connected to $\overline{A}/S$. If D7 equals 1, then semigraphics mode 4 is selected.

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OUTPUT SIGNALS

Burst (BURST)

This output signal goes high at burst time in all modes.

Burst Pseudo Color ($\overline{\text{BURSTPC}}$)

This signal has an open drain output which pulls low at burst time when the VDG is in a black-and-white mode.

Chroma Bias (CHB)

This signal is an analog output and provides a dc reference corresponding to the quiescent value of ϕA and ϕB. The CHB signal is used to guarantee good thermal tracking and minimize the variation between the MC1372 and the VDG. This signal, when pulled low, resets certain registers within the chip. In a user's system, this signal should not normally be used as an input. It is used mainly to enhance test capabilities within the factory.

Field Sync ($\overline{\text{FS}}$)

The high-to-low transition of the $\overline{\text{FS}}$ output coincides with the end of active display area (see Figures 12 and 22). During this time interval, an MPU may have total access to the display RAM without causing undesired flicker on the screen. The low-to-high transition of $\overline{\text{FS}}$ coincides with the trailing edge of the vertical synchronization pulse.

Horizontal Sync ($\overline{\text{HS}}$)

The $\overline{\text{HS}}$ pulse coincides with a horizontal synchronization pulse furnished to the television receiver by the VDG (see Figure 11). The high-to-low transition of the $\overline{\text{HS}}$ pulse coincides with the leading edge of the horizontal synchronization pulse and the low-to-high transition coincides with the trailing edge.

Phase A (ϕA)

The ϕA signal is a three-level analog output used in combination with ϕB and Y outputs to specify one of eight colors. It is used to transfer color information to a standard NTSC color television receiver via the MC1372 RF modulator (see Figures 7, 13, and 14).

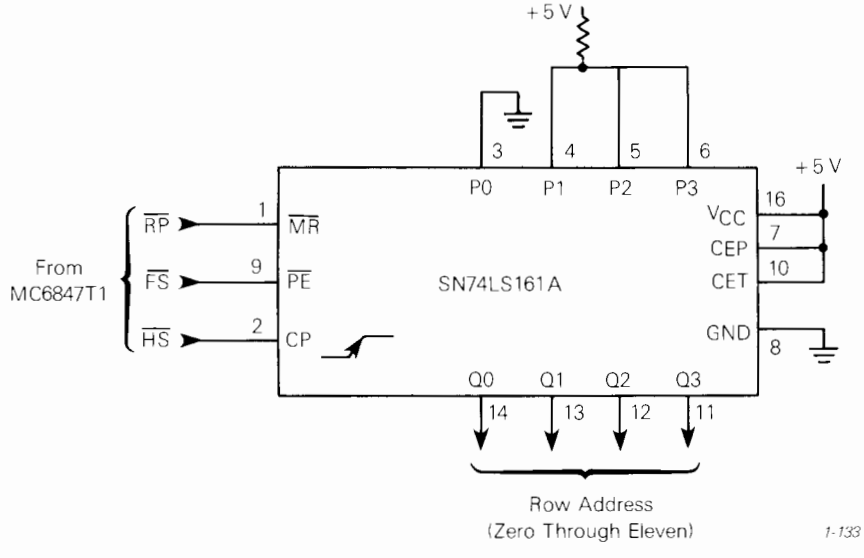
Phase B (ϕB)

The ϕB signal is a four-level analog output used in combination with ϕA and Y outputs to specify one of eight colors. The additional one analog level is used to specify the time of the color burst reference signal. It is used to transfer color information to a standard NTSC color television receiver via the MC1372 RF modulator (see Figures 7, 13, and 14).

Row Preset ($\overline{\text{RP}}$)

If desired, an external character generator ROM may be used with VDG. An external 4-bit counter must be added to supply row addresses. The counter is clocked by the $\overline{\text{HS}}$ signal and is cleared by the $\overline{\text{RP}}$ signal. The $\overline{\text{RP}}$ pulses occur in all alphanumeric and semigraphic modes; no pulses are output in the full graphic modes. The $\overline{\text{RP}}$ occurs after the first valid 12 lines. Therefore, a $\overline{\text{FS}}$-clocked preloadable counter such as a SN74LS161A shown in Figure 21 should be used.

FIGURE 21 — EXTERNAL CHARACTER GENERATOR ROW COUNTER



VDG Clock (VCLK)

The VCLK clock input signal requires a 3.579545 MHz (standard color burst) TV crystal frequency square wave. The duty cycle of this clock must be between 45% and 55% since it controls the width of alternate dots on the television screen. The SAM provides this clock. The VDG will power-up using either the rising or falling edge of the clock. The dotted line on the CLK signal in Figure 5 shows the characteristic of latching in data on either clock edge.

Luminance (Y)

This six-level analog output contains composite sync, blanking, and four levels of video luminance. It is used to transfer luminance to a standard NTSC color television receiver via the MC1372 RF modulator (see Figures 7, 13, and 14).

POWER SIGNALS

V_{CC} and V_{SS}

The V_{CC} signal supplies the power to the VDG. The V_{SS} signal is the ground connection. The NC pins are not connected and are spare pins.

OPERATION OF THE VDG

VIDEO TIMING AND CONTROL

This part of the VDG includes the mode decoding, timing generation, and associated row counter logic. It uses the 3.58 MHz color frequency to generate horizontal and vertical timing information (via linear shift register counters), which the video and chroma encoder uses to generate color video information.

The horizontal timing for the VDG is summarized in Figure 11. Ten and one-half cycles of the 3.58 MHz subcarrier are transmitted on the back porch of every horizontal blanking period. This color burst is suppressed during vertical sync. Color burst is also suppressed in the black-and-white two-color graphic modes. This can lead to some interesting rainbow effects (pseudo colors) on the display which is frequency and pattern dependent.

The vertical timing for the VDG is shown in Figure 22. After the lower border has been displayed, vertical blanking begins with the luminance output (Y) being brought to the blanking level. Three normal horizontal sync pulses on Y are followed by three vertical sync pulses. The remaining vertical blanking period contains 13 horizontal sync pulses. After vertical blanking, the upper border is displayed for 25 scan lines followed by 192 scan lines of active display. After the 192nd active scan line has been displayed, the lower border begins, lasting 26 scan lines. The lower border is followed by vertical blanking. Since the MC6847T1 VDG is non-interlaced, vertical timing between fields is identical.

INTERNAL CHARACTER GENERATOR ROM

Since many uses of the VDG will involve the display of alphanumeric data, a character generator ROM is included on the chip. The ROM will generate standard 5 × 7 dot matrix characters with true descenders within a 8 × 12 character block.

INTERNAL/EXTERNAL CHARACTER GENERATOR MULTIPLEXER

The internal/external multiplexer allows the use of either the internal ROM or an external character generator. This multiplexer may be switched on a character-by-character basis to allow mixed internal and external character generation on the display. The external character may be any desired dot pattern in the standard 8 × 12 one-character display matrix, thus allowing the maximum 256 × 192 screen density.

VIDEO AND COLOR SUBSYSTEM

The 8-bit output of the internal/external multiplexer is serialized in an 8-bit shift register clocked at the dot-clock frequency (2 × VCLK). The luminance information from the shift register is summed with the horizontal and vertical sync signals to produce a composite video signal less the chrominance information, called Y. The luminance signal, Y, and the two chrominance outputs, ϕA (R-Y) and ϕB (B-Y), can be combined (modulated) by an MC1372 into a composite video signal. Figure 13 shows the relationship between the luminance and chrominance signals and the resultant color.

DISPLAY MODES

There are two major display modes in the VDG. Major mode 1 contains four alphanumeric modes and one limited-graphic mode. Major mode 2 contains eight graphic modes: four are full color graphic and four are restricted color graphic modes. The mode selection for the VDG is summarized in Tables 4 and 5. The mnemonics of these fourteen modes is explained in the following sections.

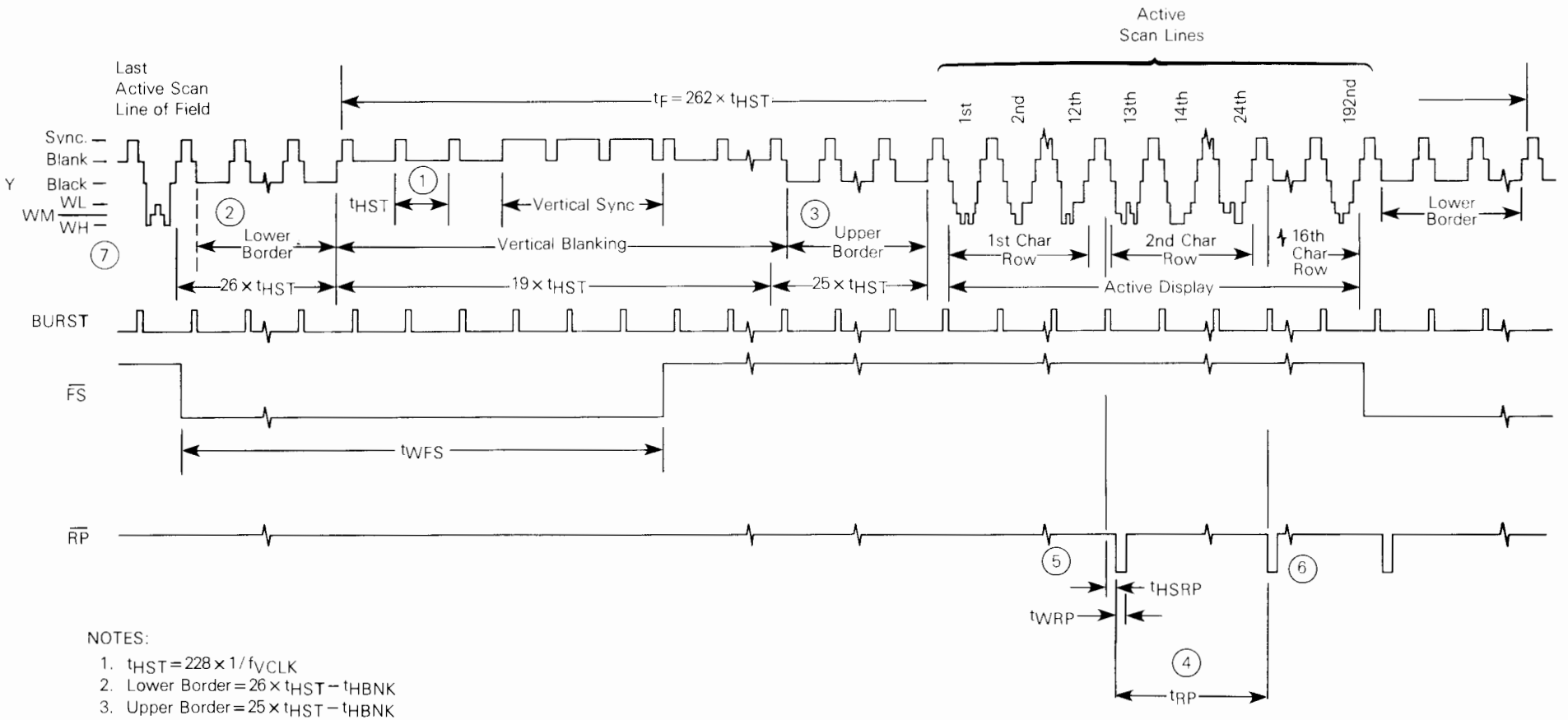
In major mode 1, the display window is divided into 32 columns by 16 character element rows thus requiring 512 bytes of memory. Each character element is 8 dot clock periods by 12 scan lines in size as shown in Figure 23. The area outside the display window depends on GM1, GM2, and $\overline{A}$/G.

The VDG has a built-in character generator ROM containing 96 ASCII characters in a 5 × 7 format (see Figure 24). The 5 × 7 character font is positioned two columns to the right and one row down within the 8 × 12 character block. This allows the lowercase characters to have true descenders. Seven bits on the 8-bit data word are typically used for the internal ASCII character generator. For a complete representation of each character, see Figure 24. The remaining bit is used to implement the semigraphics on a character-by-character basis.

If an external ROM is used, all of the 8 × 12 picture elements (or pixels) in the character element can be utilized. Characters may be either green on a dark green background or orange on a dark orange background depending on the state of the CSS signal. The screen invert function can reverse the character luminance level.

The limited-graphic mode is semigraphics 4. In semigraphics 4, the 8 × 12 dot character block is divided into four pixels (each pixel is four dot clocks by six scan lines). The four low-order bits (DD0 through DD3) of each incoming byte of data select one of sixteen possible illumination patterns while the next three bits (DD4 through DD6) determine the color of the illuminated elements. To select the

FIGURE 22 — VERTICAL TIMING



NOTES:

1. $t_{HST} = 228 \times 1/f_{VCLK}$
2. Lower Border $= 26 \times t_{HST} - t_{HBNK}$
3. Upper Border $= 25 \times t_{HST} - t_{HBNK}$
4. $t_{RP} = 12 \times t_{HST}$
5. t_{WRP} and t_{HSRP}, see Figure 11.
6. RP occurs after the 12th, 24th, 36th, ..., 192nd active scan line.
7. Voltage levels and timing are not drawn to scale.

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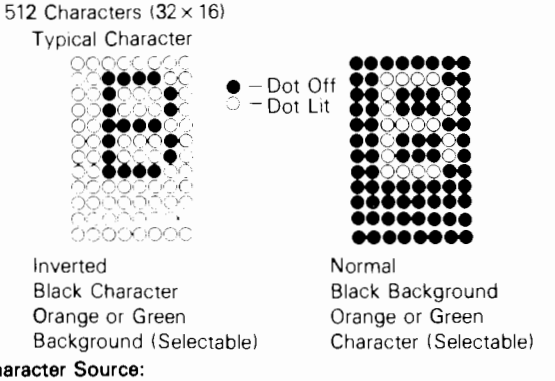
FIGURE 23 — ALPHANUMERIC MODE (INTERNAL)



Character Source:
Internal — 6 Bit ASCII Generator ROM On Chip or User Definable
External — Users ROM

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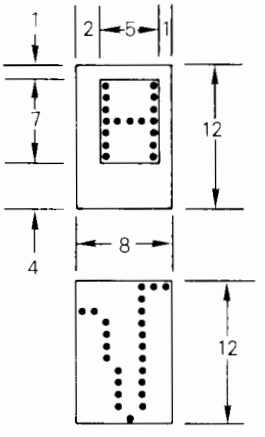
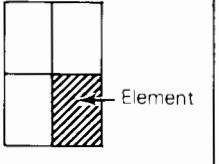
TABLE 4 — SUMMARY OF MAJOR MODES

Major Mode 1 — Alpha Modes

Title	Memory	Display Elements	Colors	Title	Memory	Display Elements	Colors
Alphanumerics (Internal)	512 × 8		2	Semigraphic 4	512 × 8		8
Alphanumerics (External)	512 × 8		2				

Major Mode 2 — Graphics Modes

Title	Memory	Colors	Comments	# of Color Sets
64 × 64 Color Graphic	1 K × 8	4	Matrix 64 × 64 Elements	2
128 × 64 Graphics*	1 K × 8	2	Matrix 128 Elements Wide by	2
128 × 64 Color Graphic	2 K × 8	4	64 Elements High	
128 × 96 Graphics*	1.5 K × 8	2	Matrix 128 Elements Wide by	2
128 × 96 Color Graphic	3 K × 8	4	96 Elements High	
128 × 192 Graphics*	3 K × 8	2	Matrix 128 Elements Wide by	2
128 × 192 Color Graphic	6 K × 8	4	192 Elements High	
256 × 192 Graphics	6 K × 8	2	Matrix 256 Elements Wide by 192 Elements Wide	2

*Graphics mode turns on or off each element. The color may be one of two.

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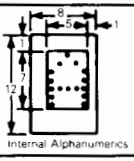
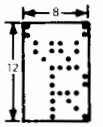
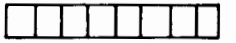
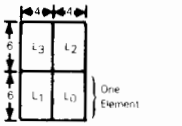
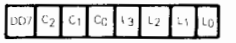
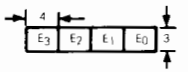
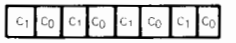
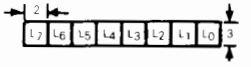
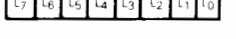
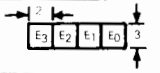
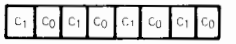
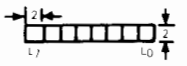
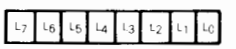
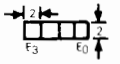
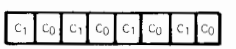
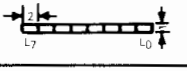
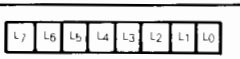
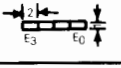
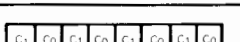
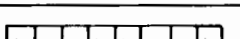
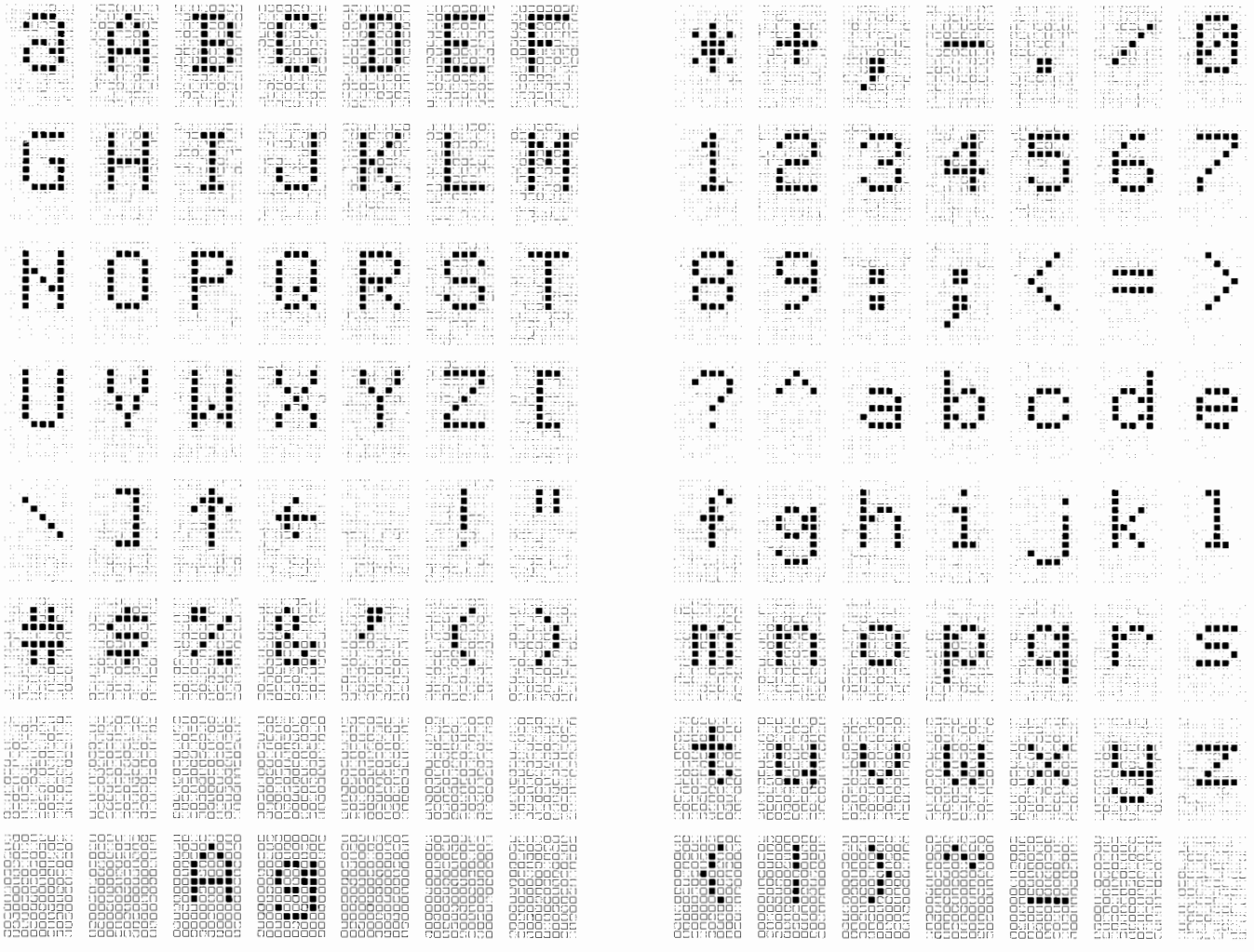
TABLE 5 — DETAILED DESCRIPTION OF VDG MODES

VDG Pins								Color			TV Screen		VDG Data Bus	Comments
A/G	DD7	EXT/INT	GM2	GM1	GM0	CSS	DD6	Character Color	Background	Border	Display Mode	Detail		
0	0 * 0 1	0	x	x *	x *	0 1	0 1 0 1 *	Green Black Orange Black	Black Green Black Orange	*	32 Characters per row 16 Characters in rows	 Internal Alphanumerics		The ALPHANUMERIC INTERNAL mode uses an internal character generator. DD7 must be low for alpha mode.
0	0	1	x	x	x	0 1	0 1 0 1	Green Black Orange Black	Black Green Black Orange	*	32 Characters per row 16 Characters in rows		 One Row of Custom Characters	The ALPHANUMERIC EXTERNAL mode uses an external character generator as well as a row counter. Thus, custom character fonts or graphic symbol sets with up to 256 different 8 x 12 dot "characters" may be displayed.
0	1	0	x	x	x	x	x	Lx C2 C1 C0 0 x x x 1 0 0 0 1 0 0 1 1 0 1 0 1 0 1 1 1 1 0 0 1 1 0 1 1 1 1 0 1 1 1 1	Color Black Green Yellow Blue Red Buff Cyan Magenta Orange	*	64 Display elements per row 32 Display elements in rows			The SEMIGRAPHICS FOUR mode uses an internal "course graphics" generator in which a rectangle (eight dots by twelve dots) is divided into four equal parts. The luminance of each part is determined by a corresponding bit on the VDG data bus. The color of illuminated parts is determined by three bits. DD7 must be high for this mode.
1	x	x	0	0	0	0 1	x	C1 C0 0 0 0 1 1 0 1 1 0 0 0 1 1 0 1 1	Color Green Yellow Blue Red Buff Cyan Magenta Orange	Green Buff	64 Display elements per row 64 Display elements			The COLOR GRAPHICS ONE mode uses a maximum of 1024 bytes of display RAM in which one pair of bits specifies one picture element.
1	x	x	0	0	1	0 1	x	Lx 0 1 0 1	Color Black Green Black Buff	Green Buff	128 Display elements per row 64 Display elements in rows			The RESOLUTION GRAPHICS ONE mode uses a maximum of 1024 bytes of display RAM in which one bit specifies one picture element.
1	x	x	0	1	0	0 1	x	Same color as Color Graphics One		Green Buff	128 Display elements per row 64 Display elements in rows			The COLOR GRAPHICS TWO mode uses a maximum of 2048 bytes of display RAM in which one pair of bits specifies one picture element.
1	x	x	0	1	1	0 1	x	Same color as Resolution Graphics One		Green Buff	128 Display elements per row 96 Display elements in rows			The RESOLUTION GRAPHICS TWO mode uses a maximum of 1536 bytes of display RAM in which one bit specifies one picture element.
1	x	x	1	0	0	0 1	x	Same color as Color Graphics One		Green Buff	128 Display elements per row 96 Display elements in rows			The COLOR GRAPHICS THREE mode uses a maximum of 3072 bytes of display RAM in which one pair of bits specifies one picture element.
1	x	x	1	0	1	0 1	x	Same color as Resolution Graphics One		Green Buff	128 Display elements per row 192 Display elements in rows			The RESOLUTION GRAPHICS THREE mode uses a maximum of 3072 bytes of display RAM in which one bit specifies one picture element.
1	x	x	1	1	0	0 1	x	Same color as Color Graphics One		Green Buff	128 Display elements per row 192 Display Elements in rows			The COLOR GRAPHICS SIX mode uses a maximum of 6144 bytes of display RAM in which one pair of bits specifies one picture element.
1	x	x	1	1	1	0 1	x	Same color as Resolution Graphics One		Green Buff	256 Display elements per row 192 Display elements in rows			The RESOLUTION GRAPHICS SIX mode uses a maximum of 6144 bytes of display RAM in which one bit specifies one picture element.

* See Table 1 and Figure 20.

FIGURE 24 — CHARACTER ROM PATTERN



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semigraphic 4 mode, DD7 must be high. Figure 25 shows the color and pattern selections for semigraphic modes.

The display window in major mode 2 (full graphics) has a less rigorous format than in major mode 1. The display elements vary from one scan line to three scan lines in height. The length of the display element is either eight or sixteen half-periods wide. Each display element is divided into four or eight pixels. Major mode 2 corresponds to a full color mode while major mode 1, which corresponds to a restricted color mode like the semigraphics mode, represents illumination data.

When the pixel is turned on, it is illuminated with the color chosen by the color set select (CSS) signal. When the pixel is turned off, it is black. In the full color modes, pairs of data bits choose one of four colors in one of two color sets defined by the CSS signal. Depending on the state of the CSS signal, the area outside the display window is either green or buff. The display formats and color selection for major mode 1 (alphanumeric) are summarized in Figure 23.

The 64 × 64 Color Graphics 1 Mode (CG1)

The 64 × 64 color graphics mode generates a display matrix of 64 elements wide by 64 elements high. Each element may be one of four colors with two color sets possible (selected by CSS). A 1K × 8 display memory is required. The display RAM is accessed 16 times per horizontal line. Each element equals four dot clocks by three scan lines.

The 128 × 64 Resolution Graphics 1 Mode (RG1)

The 128 × 64 graphics mode generates a matrix 128 elements wide by 64 elements high. Each element may be either ON or OFF. However, the entire display may be one of two colors selected by using the CSS signal. A 1K × 8 display memory is required. The display RAM is accessed 16 times per horizontal line. Each element equals two dot clocks by three scan lines. The ϕB burst is absent when CSS equals one.

The 128 × 64 Color Graphics 2 Mode (CG2)

The 128 × 64 color graphics mode generates a display matrix 128 elements wide by 64 elements high. Each element may be one of four colors with two color sets possible selected by CSS. A 2K × 8 display memory is required. The display RAM is accessed 32 times per horizontal line. Each element equals two dot clocks by three scan lines.

The 128 × 96 Resolution Graphics 2 Mode (RG2)

The 128 × 96 graphics mode generates a display matrix 128 elements wide by 96 elements high. Each element may be either ON or OFF. The entire display may be one of two colors selected by using the CSS signal. A 1.5K × 8 display memory is required. The display RAM is accessed 16 times per horizontal line. Each element equals two dot clocks by two scan lines. The ϕB burst is absent when CSS equals one.

The 128 × 96 Color Graphics 3 Mode (CG3)

The 128 × 96 color graphics mode generates a display matrix 128 elements wide by 96 elements high. Each element may be one of four colors with two color sets possible selected by CSS. A 3K × 8 display memory is required. The display RAM is accessed 32 times per horizontal line. Each element equals two dot clocks by two scan lines.

The 128 × 192 Resolution Graphics 3 Mode (RG3)

The 128 × 192 graphics mode generates a display matrix 128 elements wide by 192 elements high. Each element may be either ON or OFF. However, the ON element may be one of two colors selected by using the CSS signal. A 3K × 8 display memory is required. The display RAM is accessed 16 times per horizontal line. Each element equals two dot clocks by one scan line. The ϕB burst is absent when CSS equals one.

The 128 × 192 Color Graphics 6 Mode (CG6)

The 128 × 192 color graphics mode generates a display matrix 128 elements wide by 192 elements high. Each element may be one of four colors with two color sets possible (selected by CSS). A 6K × 8 display memory is required. The display RAM is accessed 32 times per horizontal line. Each element equals two dot clocks by one scan line.

The 256 × 192 Resolution Graphics 6 Mode (RG6)

The 256 × 192 graphics mode generates a display matrix 256 elements wide by 192 elements high. Each element may be either ON or OFF. However, the ON element may be one of two colors selected by using the CSS signal. A 6K × 8 display memory is required. The display RAM is accessed 32 times per horizontal line. Each element equals one dot clock by one scan line. The ϕB burst is absent when CSS equals one.

ASSOCIATED DEVICES

SN74LS783/SN74LS785 — Synchronous Address Multiplexer (SAM)

The SAM, a digital bipolar companion to the MC6800 or MC6809E (external clock input), is primarily a VDG transparent-access controller. It allows the microprocessor to read and store to VDG display memory ("screen RAM") without waiting for a blank screen interval. Figure 2 shows a typical system using the SAM and the MC6809E.

The inherent interleaved direct memory access (IDMA), which occur continuously, keep (1) the VDG updated with the proper data (independent of mode) and (2) the dynamic memory (used as a system memory with the SAM) refreshed. This is also done through a IDMA process during the time the VDG does not need display data (horizontal and vertical sync times).

In addition to being a transparent memory access and dynamic memory controller, the SAM also functions as an external clock generator for the MC6800/MC6809E (slight additional circuitry is required for the MC6800).

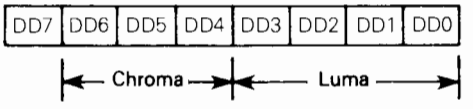
MC1372/MC1373 Chroma/RF Modulator

The MC1372 is a chrominance phase-shift modulator with built-in RF up-converter. The part may be used without the RF modulator for chroma only or the RF oscillator may be defeated and composite chrominance and luminance can be obtained (see Figure 27).

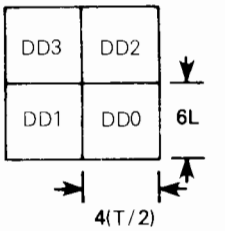
The MC1373 is an RF modulator only (similar to the second half of the MC1372) and can be used to up-modulate separate luma and chroma signals at the receiver for high quality video reception.

FIGURE 25 — SEMIGRAPHIC MODE ENCODING

(a) Data and Display Formats



Semigraphics 4



Luma DN	SG4			Color
	DD6	DD5	DD4	
0	X	X	X	Black
1	0	0	0	Green
1	0	0	1	Yellow
1	0	1	0	Blue
1	0	1	1	Red
1	1	0	0	Buff
1	1	0	1	Cyan
1	1	1	0	Magenta
1	1	1	1	Orange

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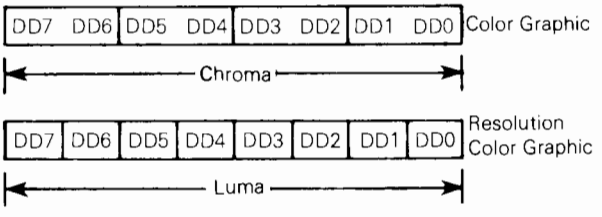
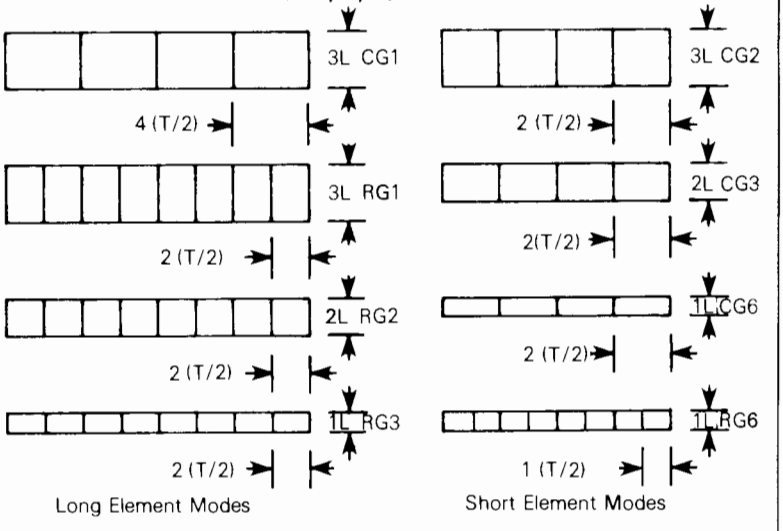
FIGURE 26 — GRAPHIC MODE ENCODING

(a) Data Format



(b) Display Format



Long Element Modes

Short Element Modes

(c) Color Selection

CSS	Border	Resolution Color Mode		Color Mode		
		D_N	Color	D_N+1	D_N	Color
0	Green	0	Black	0	0	Green
0	Green	1	Green	0	1	Yellow
0	Green	1	Green	1	0	Blue
0	Green	1	Green	1	1	Red
1	Buff	0	Black	0	0	Buff
1	Buff	1	Buff	0	1	Cyan
1	Buff	1	Buff	1	0	Magenta
1	Buff	1	Buff	1	1	Orange

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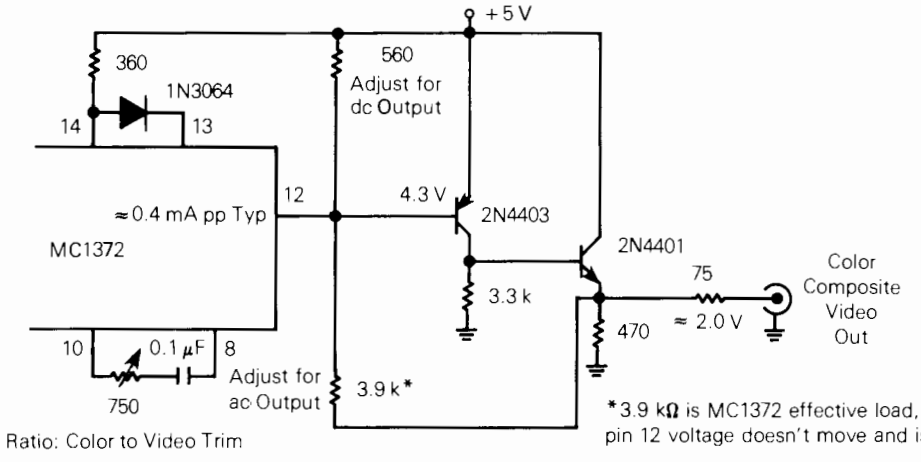
FIGURE 27 — COLOR COMPOSITE VIDEO TO COLOR MONITOR



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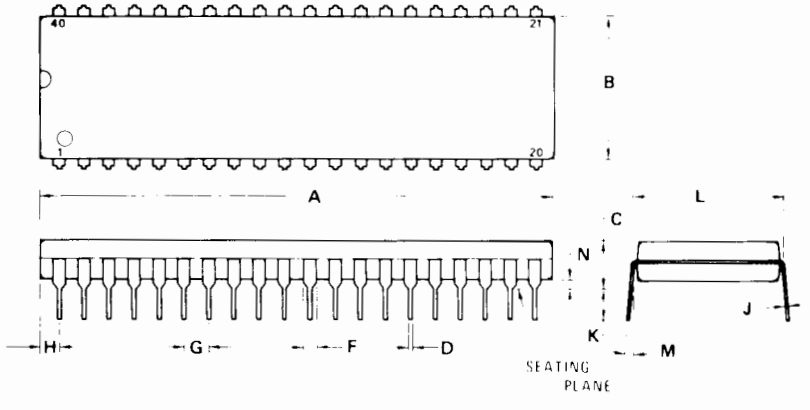
MECHANICAL DATA

P SUFFIX
PLASTIC PACKAGE
CASE 711-03

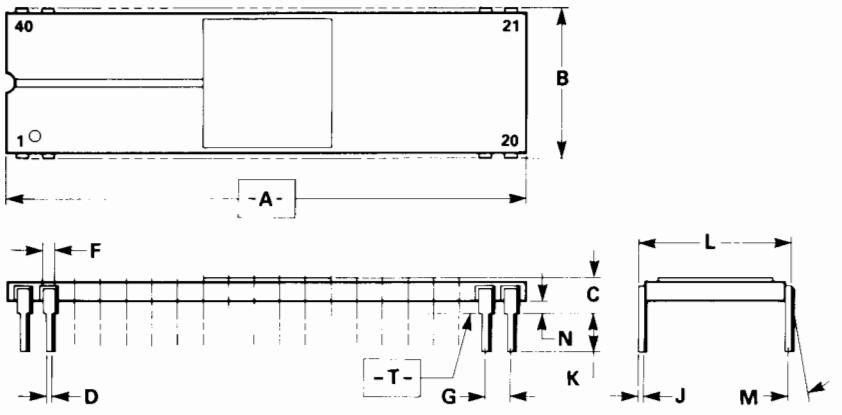


DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.69	52.45	2.035	2.065
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

MECHANICAL DATA (CONTINUED)

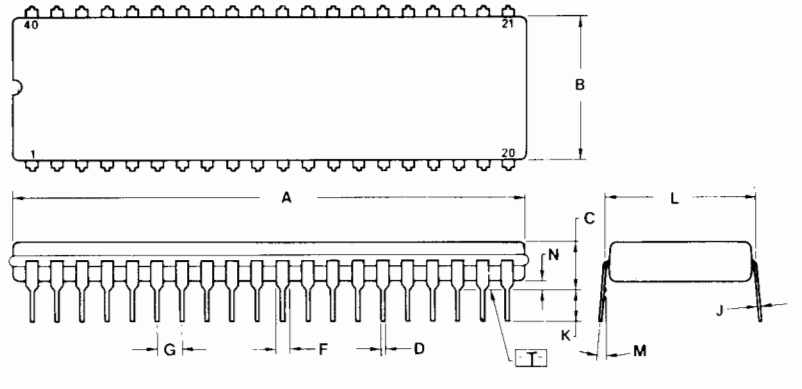
L SUFFIX
CERAMIC PACKAGE
CASE 715-05



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	50.29	51.31	1.980	2.020
B	14.63	15.49	0.576	0.610
C	2.79	4.32	0.110	0.170
D	0.38	0.53	0.015	0.021
F	0.76	1.52	0.030	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.33	0.008	0.013
K	2.54	4.57	0.100	0.180
L	14.99	15.65	0.590	0.616
M	—	10°	—	10°
N	1.02	1.52	0.040	0.060

NOTES:
1. DIMENSION -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   Ⓟ 0.25 (0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

S SUFFIX
CERDIP PACKAGE
CASE 734-04



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	51.31	53.24	2.020	2.096
B	12.70	15.49	0.500	0.610
C	4.06	5.84	0.160	0.230
D	0.38	0.56	0.015	0.022
F	1.27	1.65	0.050	0.065
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM -A- IS DATUM.
2. POSITIONAL TOLERANCE FOR LEADS:
   Ⓟ Ø 0.25(0.010) Ⓜ T A Ⓜ
3. -T- IS SEATING PLANE.
4. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
5. DIMENSIONS A AND B INCLUDE MENISCUS.
6. DIMENSIONING AND TOLERANCING PER ANSI Y14.5, 1973.

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